DESIGN AND FABRICATION OF PN SEQUENCE GENERATOR AND CORRELATOR FOR RAKE SYSTEM

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C E R T I F I C A T E

Certified that this work " Design and Fabrication of PN sequence Generator and Correlator for Rake System" by Mr. K.N. Hari Bhat has been carried out under our supervision and that this has not been submitted elsewhere for a degree.

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C O N T E N T S

CHAPTER I

INTRODUCTION

Rake as a communication system to combat against fading and intersymbol interference has been discussed by Price and Green[1]. Here the multipath components are isolated by correlation technique at the receiver, by using wideband noise coded signal for mark and space. These components are added, after applying a weighting coefficient derived from the channel measurement and introducing a delay so that they are brought to phase. Rake technique can also be incorporated to find the randomly varying inphase and quadrature components of $g(t, \xi_t)$ (linear time varying impulse response of the channel). From a record of $g(t, \xi_t)$ the multipath structure and Doppler shifts can be obtained. It is also possible to calculate scattering function which gives the distribution of received signal energy as a functio of multipath time delay and Doppler frequency shift. Channel sounding experiments have been successfully conducted using Rake Technique by Barrow[2] and Berkimier[3].

In this report ~~in Chapter II~~ description and characterisation of tropochannels are presented. It ~~Chapter III~~ deals with the channel sounding experiments using Rake technique. Two types of existing Rake systems and the proposed scheme are given.

Generation of wide band noise like signal (PN sequence) using shift registers, properties of such a signal and hardware design ~~is~~ are considered in Chapter IV.

Chapter V is devoted to description, design and working of current switch.

Chapter VI concludes the thesis.

References:

1. Price R and P.E. Green Jr., " A Communication Technique for Multipath channels" Proc.IRE Vol 46 pp 555-570 March 1958.

2. Barrow B.B., et al "Indirect Atmospheric Measurements Utilising Rake Troposcatter Techniques Part I." Proc. IEEE Vol 57 pp 537-551 April 1969.

3. Birkemeier, W.P. et al; " The Identification of atmospheri Refractivity Structure Using Forward Scatter Rake Techniques", Lecture notes of the Intensive Course on Digital Communication Via Fading Channels IIT Kanpur March 1972.

CHAPTER II

In this chapter a brief description of tropospheric propagation, tropochannel model and mathematical relationships are dealt.

2-1 Tropospheric propagation: Troposphere is the region above the earth which can be used as a channel for transmission of microwaves in the UHF or SHF bands, between two points, located on earth's surface, seperated by a distance of about 70 to 600 miles. Such a system using high power and large directional antennas, can surmount ground obstacles, provide high grade multichannel service and high propagational reliability. It has unique advantages in inhospitable terrain where other methods of communication is impractical. It also provides an excellant spectrum ulilisation and offers a high degree of security compared to other methods of communication.

A communication system based on tropospheric propagation utilises the scattering of electromagnetic waves due to atmospheric turbulance. The turbulence produces blobs of atmosphere whose refractive indeces are different from the surrounding medium. When a microwave signal is transmitted, the signal is scattered in all directions by these blobs. The scattered components which are in the forward direction produce a field at the receiving

station. Thus the propagation medium contains several paths from the transmitter to the receiver. Different layers of scatterers give rise to different electrical path lengths and hence the components arriving through these paths have different propagation times. The loci of all scatterers which give rise to identical propagation time form an ellipsoid with transmitting and receiving antenna phase centres as foci. The random motion of scatterers cause the components (echo) from various paths to arrive at the receiver at randomly varying delays and amplitudes. The total received signal is a vector sum of individually delayed signals. If we consider a single tone type of transmitted signal of the form A sin $w_c t$, the received signal is

$$R(t) = \sum_{i=1}^{m} A_i(t) \text{ Sin } (w_c t + \Phi_i(t)) \quad \ldots\ldots (2\text{-}1)$$

where m is no. of scatterers. $A_i(t)$ and $\Phi_i(t)$ are random processes. The amplitude and phase of the received signal thus varies with time over a given channel . These can be separated into short term (over a period shorter than a few minutes) and long term (hourly median levels over a longer time e.g. a month or a year) variations.
In short periods the amplitude variations are described by Rayleigh distribution and the phase is uniformly distributed.

Thus the probability density of envelop of R(t) is given by

$$p_R(r) = \frac{r}{\sigma^2} e^{-r^2/2\sigma^2} \qquad r \geq 0 \qquad (2\text{-}2)$$

and the probability density $p_\Phi(\theta)$ of phase of R(t) is given by

$$p_\Phi(\theta) = \frac{1}{2\pi} \qquad -\pi < \theta < \pi$$

2-2 Model of Tropochannel: The tropochannel can be considered to be a linear time varying band pass filter the impulse response of which is a Ganssian process. Let z(t) be the complex envelope of the signal input, $g(t, \xi)$ complex equivalent low pass impulse response of such a filter (response at time t due to an impulse at time $(t - \xi)$. Then complex low pass signal output w(t) is

$$w(t) = \int_{-\infty}^{\infty} g(t, \xi) \, z(t-\xi) \, d\xi \qquad (2\text{-}3)$$

This equation leads to a model in which $g(t, \xi) \, d\xi$ is the complex gain produced by stationary scatterers that give rise to delays in the range $(\xi, \xi + d\xi)$. This is illustrated in fig (2-1) with a densly tapped delay line.

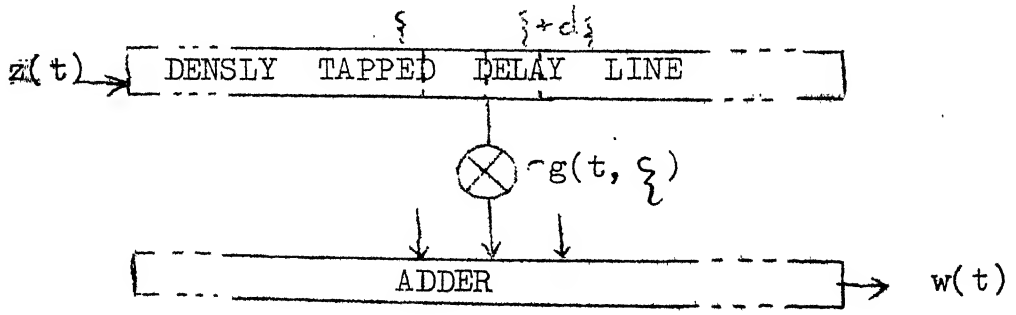


Fig. 2-1.Densly Tapped Delay Line Model.

If $z(t)$ is band limited to $-W/2 < f < W/2$ then from sampling theorem

$$z(t) = \sum_{m=-\infty}^{\infty} z\left(\frac{m}{W}\right) \frac{\sin W\left(t - \frac{m}{W}\right)}{W\left(t - m/W\right)} \qquad - (2\text{-}4)$$

Further when the input and outputs of a wide band filter are so chosen as to lie in a narrow bandwidth with the same centre frequency, we can replace the wideband filter with an equivalent narrow band filter.

The lowpass time variant transfer function of the channel is given by

$$T(t, f) = \int_{-\infty}^{\infty} g(t, \xi)\, e^{-j 2\pi f \xi}\, d\xi \qquad \ldots. (2\text{-}5)$$

This is also a zero mean Gaussian process. If the signal is bandlimited to $-W/2 < f < W/2$ the equivalent lowpass timevariant transfer function band limited to $-W/2 < f < W/2$ is

$$T_E(t, f) = \begin{cases} T(t,f) & |f| < W/2 \\ 0 & |f| > W/2 \end{cases} \qquad \ldots (2\text{-}6)$$

and the equivalent lowpass time varying impulse response for the channel corresponding only to its lowpass transfer function band limited to $-w/2 < f < w/2$ is

$$g_E(t,\xi) = \int_{-\infty}^{\infty} T_E(t, f)\, e^{j 2\pi f \xi}\, df \qquad (2\text{-}7)$$

From Eqns.(2-3)&(2-4) we can show that

$$w(t) = \frac{1}{W} \sum_{m=-\infty}^{\infty} g_E\left(t, m/_W\right) z\left(t - m/_W\right) \quad ..(2\text{-}8)$$

From eqn. (2-8) we see that with signals band limited to $-w/_2 < f < w/_2$, it is enough if we consider effective impulse response $g_E(t,\xi)$ at intervals of $\frac{1}{W}$. Putting $g(t, \xi_m) = \frac{1}{W} g_E(t, \frac{m}{W})$ ... (2-9)

and from Eqn. (2-8), we arrive at the tapped delay line model of the tropochannel given in fig. (2-2).

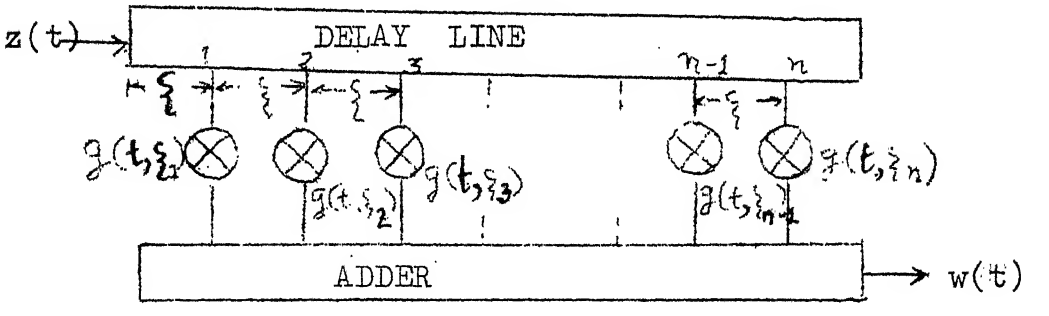


Fig. (2-2)
Tapped delay line model of Tropochannel

If we consider short term fading where the amplitude is Rayleigh distributed then $g(t, \xi_i)$, i= 1,2..n

and hence w(t) are zero mean complex Gaussian processes with identical quadrature components.

The tapgain correlation function (or multipath time covariance function) of WSS (wide sense stationary) channel is defined as

$$Q(\xi, \eta, \tau) = \overline{g^*(t, \xi)\, g(t+\tau, \eta)} \quad \ldots (2\text{-}10)$$

For a WSSUS (wide sense stationary uncorrelated scattering) channel it is of the form

$$Q(\xi, \eta, \tau) = Q(\xi, \tau)\ \delta(\xi - \eta) \quad \ldots (2\text{-}11)$$

$Q(\xi, 0)$ is called the delay power spectrum or multipath intensity profile. It gives the intensity of the scattering or reflection process at relative propagation delay ξ. Fourier transform of tapgain correlation function is called scattering function. For a WSSUS channel it is given by

$$S(\xi, \vartheta) = \int_{-\infty}^{\infty} Q(\xi, \tau)\, e^{-j\pi 2\vartheta\tau}\, d\tau \quad \ldots (2\text{-}12)$$

$S(\xi, \vartheta)$ describes the relative intensity of all scatterers whichgive rise to a propagation path of relative delay ξ and Doppler shift ϑ.

In channel sounding experiments using Rake System, the interest is to get a continuous record of quadrature components of $g(t, \xi_i)$. From these data, the tapgain correlation function, delay power spectrum and scattering function can be obtained.

References:

1. F.A. Gunther: " Tropospheric Scatter Communications Past, Present And Future" IEEE Spectrum pp 79-100 September 1966.

2. P.A. Bello: "Characterisation of Randomly Time Variant Linear Channels" IEEE Transaction on Communication Systems pp 360-393 Dec. 1963.

3. M. Schwartz, W.R. Bennett and S. Stein "Communication Systems and Techniques" McGraw Hill 1966.

4. Reference 2 Chapter I.

CHAPTER III

CHANNEL SOUNDING

In this chapter channel measurements using Rake technique are considered. Two existing Rake systems and the proposed scheme are given.

3-1. Rake System: Rake as a communication system is designed to work against the combination of random multipath and additive noise disturbances. This has been proposed by Price and Green . It is shown by Bello that at high data rates other modem techniques improve system performance. For developing the optimum modem techniques the channel characteristics are to be known which is obtained by channel sounding.

In channel sounding experiments, using Rake principle, the interest is to get a continuous record of quadrature components of channel inpulse response $g(t, \xi)$ and to investigate the fluctuations in signal amplitude and phase caused by fading. From this data it is also possible to observe multipath structure, Doppler shifts and calculate the scattering function which adequately characterise the tropochannel.

Very short periodic pulses spaced sufficiently apart so that the multipath response die out between successive pulses, can be used for channel sounding.

The disadvantage is high peak to average power ratio. In a rake system this is overcome by using a constant amplitude signal; a radio frequency carrier that is pseudorandomly modulated in phase by a PN sequence obtained from a PN seqence generator.

The transmitter in a Rake System consists of mainly

(i) a highly stable oscillator from which other desired frequencies are synthesised.

(ii) PN sequence generator

(iii) Phase modulator

(iv) Bandpass filter.

The receiver consists of

(i) highly stable oscillator (synchronised with the transmitter oscillator) and frequency synthesiser.

(ii) Mixer

(iii) IF amplifier

(iv) Demodulator

(v) PN sequence generator

(vi) Two correlators at each Rake tap one for estimating inphase and the other for quadrature component of $g(t, \xi)$.

At the receiver the received signal is demodulated to get the inphase and quadrature components. This can be achieved by using the arrangement given in Fig. 3-1 (see appendix)

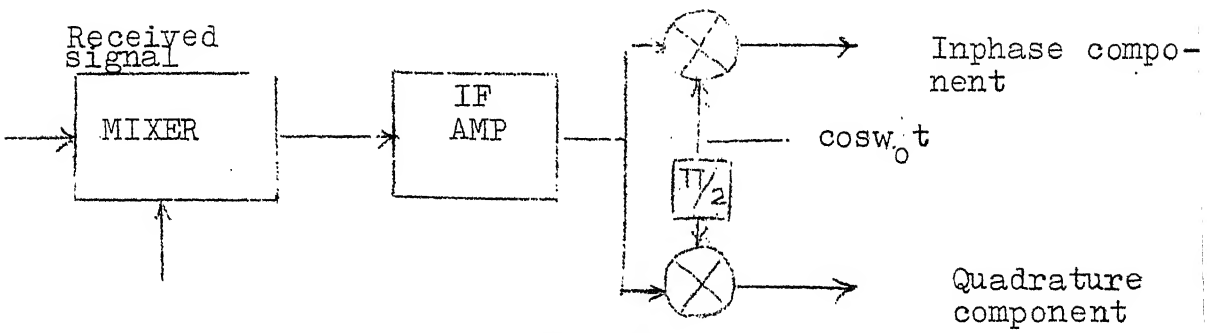


Fig. 3-1

After seperating the inphase and quadrature components of the received signal it is cross correlated with the ζ_l shifted version of the PN sequence.

Considering a segment of transmitted PN sequence $z(t)$ of duration T ($T \gg \frac{1}{W}$). Since the signal is band limited, from eqn. 2-8 and 2-9, the inphase component of the received signal $w_i(t)$ can be represented as

$$w_i(t) = \sum g_i(t, \zeta_m)\ z\left(t - \frac{m}{W}\right) \qquad 0 < t \leq T \qquad (3\text{-}4$$

where $g_i(t, \zeta_m)$ is the inphase component of $g(t, \zeta_m)$. A replica of the PN sequence delayed by k/W is available at the k^{th} tap of the receiver (Fig.3-2) which is cross correlated against $w_i(t)$ to get

$$s_{ki} = \int_{k/W}^{T+k/W} z^*\,(t - k/W)\; w_i(t)\; dt \qquad \ldots\ldots\ldots \quad (3\text{-}5)$$

$$= \sum_{m=1}^{\infty} g_i(t, \zeta_m) \int_{k/W}^{T+k/W} z^*\,(t - k/W)\; z(t - m/W)\; dt \qquad (3\text{-}6)$$

$g(t, \zeta_m)$ is assumed to remain constant over the integration period which is approximately equal to the period of the PN sequence. If $T \gg \frac{1}{W}$ the finite length integral can be approximated by its average over the ensemble of all possible T length segmentsof z(t) which gives

$$R(\tau) = \frac{1}{T}\int_0^T z^*\,(t)\; z\,(t+\tau)\; dt. \qquad (3\text{-}7)$$

The shifted version of PN sequences has autocorrelation function, $R(\tau) = -1$ for all $\tau \neq 0$ and $R(0) = 2^n - 1$, where n is number of shift register stages. (The generation&properties of PN sequence are dealt in chapter IV). Hence s_{ki} reduces to

$$s_{ki} \cong g_i\,(t, \zeta_k)\; R(0) \qquad \ldots\ldots \quad (3\text{-}8)$$

Similarly we can get $s_{kq} \cong g_g\,(t, \zeta_k)\; R(0)$ ...(3-9)

s_{ki} and s_{kq} give an estimate of inphase and quadrature component of k^{th} tapgain respectively.

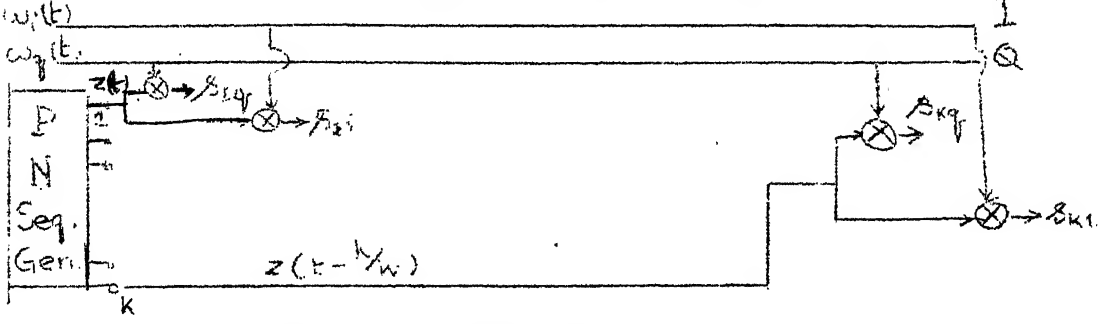


Fig. 3-2. Rake Taps.

3-2 Sylvania Rake

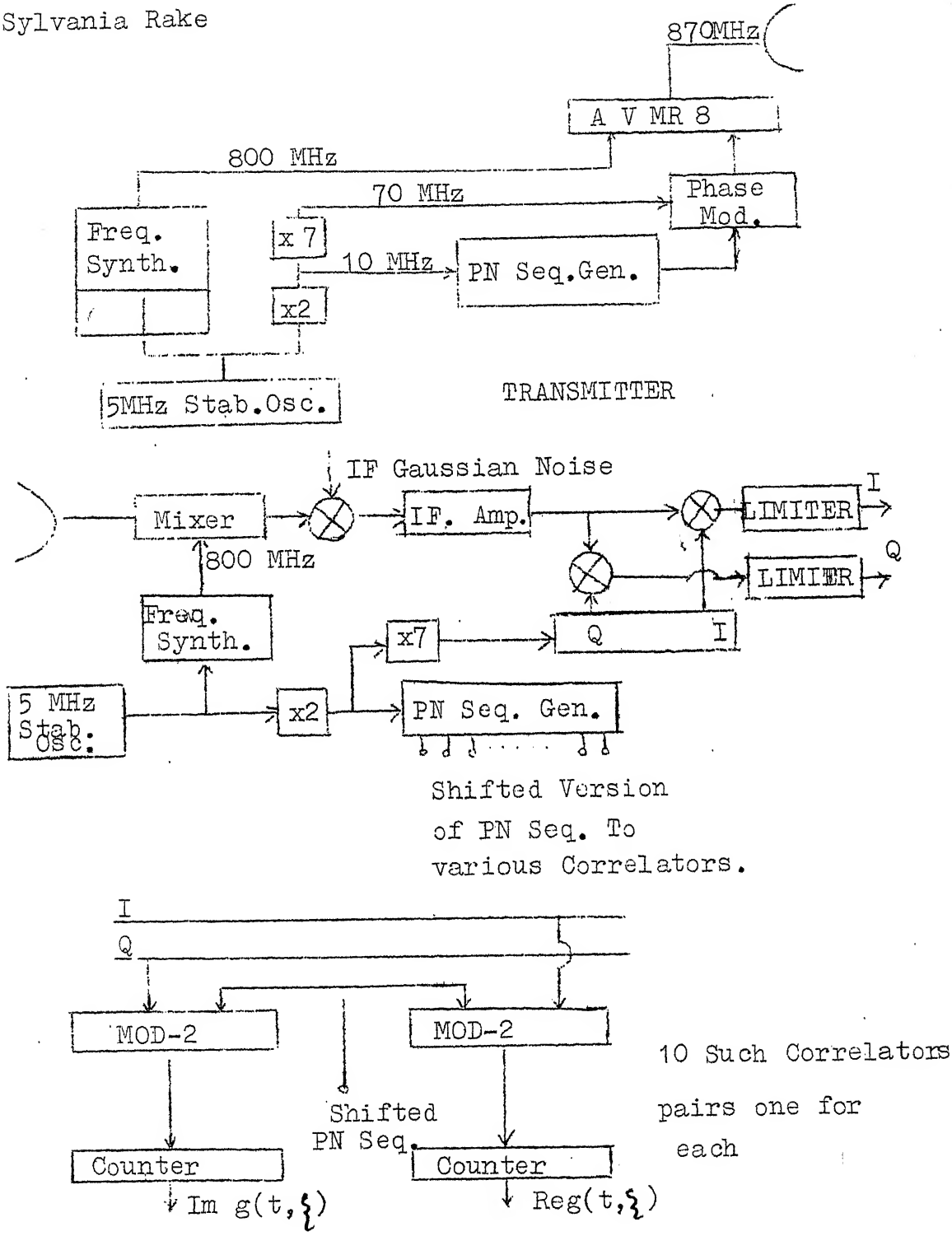
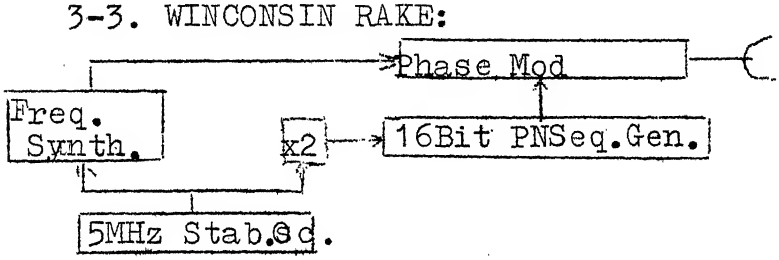


Fig. 3-3 Transmitter And Receiver of Sylvania Rake System

In this system the signal processing is done digitally. The transmitter and Receiver block diagrams are given in fig. 3-3. A 5 MHz high stability oscillator synthesises all the frequencies required. The PN sequence is obtained from a 10 stage shift register at 10 MHz clock rate. The phase modulated carrier is transmitted at 870 MHz with 10 MHz band width.

After demodulation the quadrature and inphase components of the signal are obtained in binary form. The components are then cross correlated with the ξ shifted version of PN sequence by bit by bit mod-2 addition and counting, at the ten Rake taps. The output of the m^{th} pair of counters give the estimate of the components of channel response $g(t, \xi_m)$ corresponding to the delay $m\xi$. Barrow has shown that the counter output gives minimum error estimate of $g(t, \xi)$ under low SNR conditions of the received signal. Hence Gaussian noise is added deliberately at the IF stage. The dynamic range of this Rake system is about 20 db.

3-3. WINCONSIN RAKE:



TRANSMITTER

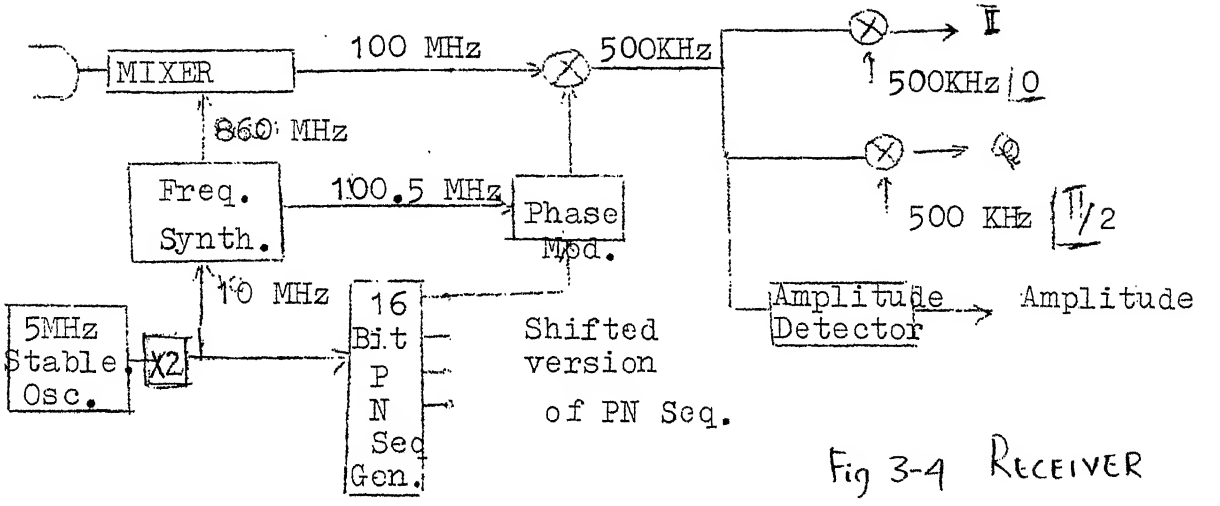


Fig 3-4 Receiver

The transmitter and receiver block diagrams are givenin Fig.3-4 . This system employs entirely analog signal processing. with good gain stability and frequency stabilities the dynamic range is about 80 db.

3-4 Proposed Scheme:

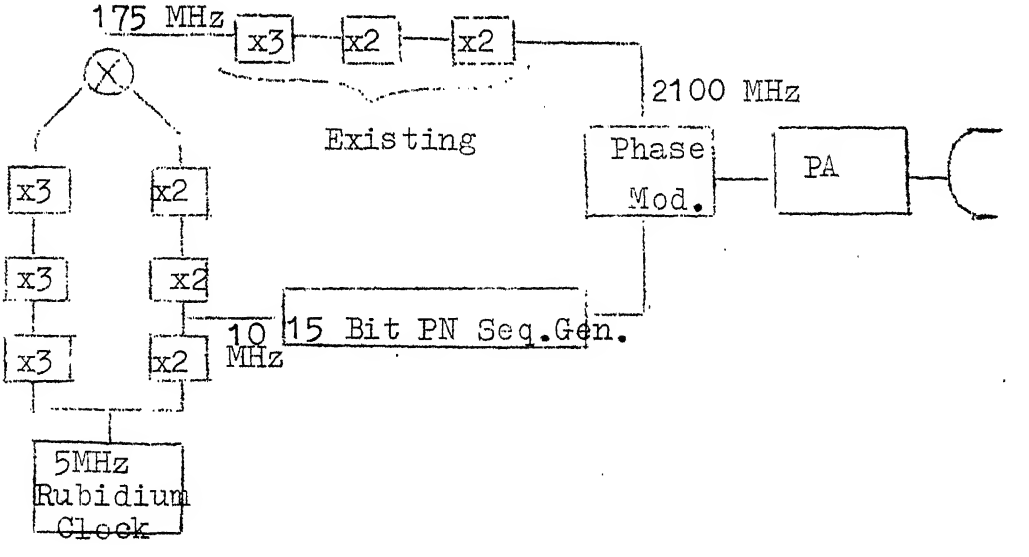
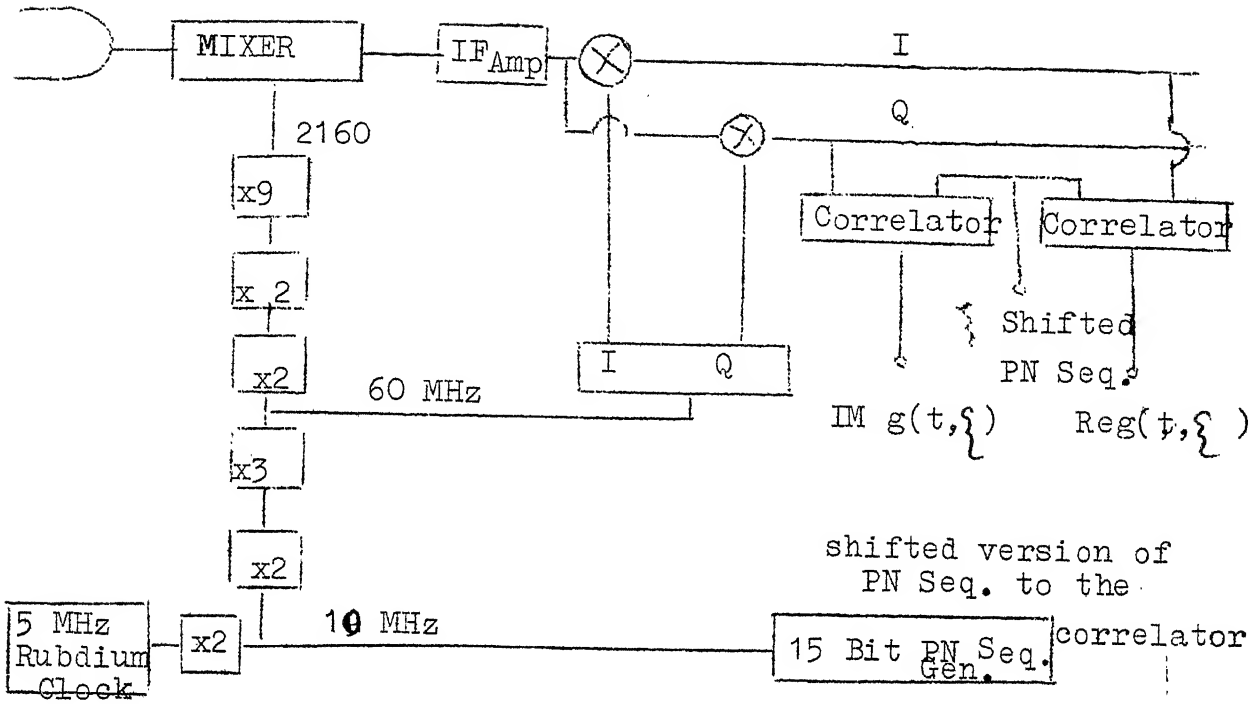


Fig. 3-5 TRANSMITTER



RECEIVER

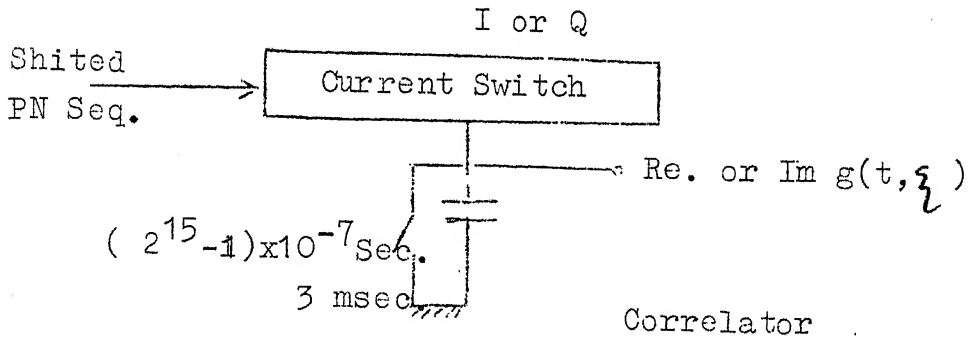


Fig. 3-5 Transmitter Receiver and Correlator

The transmitter and receiver diagram is given in Fig. 3-5. The synchronisation between transmitter and receiver is achieved by using 5 MHz Rubidium clock from which all the other desired frequencies are synthesised. These clock frequencies are periodically checked. Part of the hardware which can be used from the already existing transmitter, is incorporated . 15 Bit shift register generates the PN sequence which is transmitted at 10 Mega baud rate after phase modulation. The final carrier frequency is 2100 MHz.

At the receiver the received signal is heterodyned with 2160 MHz to get IF of 60 MHz which is then resolved into inphase and quadrature components by product demodulation. These are then cross correlated with the shifted version of the reference PN sequence at 15 Rake taps having two correlators at each tap one for inphase and one for quadrature component. The correlation is achieved by using current switch which is the heart of the system. The system description, working and hardware design of current switch is given in Chapter V. In this system the signal processing is done throughout in the analog mode. The expected dynamic range is 80 db.

References:

1. Ref. 1 Chapter I.

2. B.B. Barrow et al, " Troposcatter Propagation Tets Using Rake Receiver", Sylvania Elec. Systems Rpt. No. 461, 1965.

3. Ref. 3 Chapter I.

4. ACES Progress Report No.3 Oct 72 to March 73 IIT-Kanpur.

Appendix 3

1. Seperation of inphase and quadrature components of a complex signal: (Fig. 3-1)

Considering a modulated signal with carrier frequency w_0 of the form

$$a(t) = \rho(t)\left\{\cos\left[\omega_0 t + \phi(t)\right]\right\} \quad (1)$$

$$= \mathrm{Re}\left[u(t)e^{jw_0 t}\right] \quad (2)$$

where $u(t) = \rho(t)\, e^{j\phi(t)}$ is the complex envelope of the signal

$$u(t) = \rho(t)\cos\phi(t) + j\rho(t)\sin\phi(t) \quad (3)$$

$$= u_i(t) + j\,u_q(t) \quad (4)$$

$u_i(t)$ is the inphase component and $u_q(t)$ quadrature component of the complex envelope of $a(t)$

From eqns. (2) and (4) we have

$$a(t) = u_i(t)\ \cos w_0 t - u_q(t)\sin w_0 t$$

These components can be separated by synchronous detection with $\cos w_0 t$ and $\sin w_0 t$ as the local reference carriers.

Thus the product $a(t)\cos w_0 t$ gives $u_i(t)$ and $a(t)\sin w_0 t$ gives $u_q(t)$ after passing through the low pass filter.

CHAPTER IV

PN SEQUENCE GENERATOR

In this Chapter a brief account of Pseudo Noise (PN) sequence, its hardware realisation and testing are given.

4-1. The PN sequence is a binary sequence obtained from shift registers with suitable feedback connections. The feedback logic is obtained from the characteristic polynominal of the matrix which relates the successive states of the shift register. Considering a 3 bit shift register shown in Fig. 4-1, the states of the network is completely

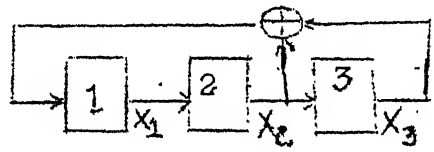


Fig. 4-1.

described by the shift register outputs X_1 X_2 and X_3 at any time. The inputs X_1^1, X_2^1 ,& X_3^1 to the shift register, becomes the next value of the shift register outputs. These inputs may be expressed as mod - 2 sums of the present outputs of the shift registers by means of a system of linear equations.

$$\left.\begin{aligned} X_1^1 &= 0 + X_2 + X_3 \\ X_2^1 &= X_1 + 0 + 0 \\ X_3^1 &= 0 + X_2 + 0 \end{aligned}\right\} \quad \ldots \quad (4\text{-}1)$$

These equations can be expressed in matrix form

$$\begin{bmatrix} X_1^1 \\ X_2^1 \\ X_3^1 \end{bmatrix} = \begin{bmatrix} 0 & 1 & 1 \\ 1 & 0 & 0 \\ 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} X_1 \\ X_2 \\ X_3 \end{bmatrix} \quad \ldots\ldots (4\text{-}2)$$

or symbolically as

$$X^1 = TX \quad \ldots\ldots\ldots \quad (4\text{-}3)$$

where X stands for the present state of the shift register. X^1 stands for the next state and T represents the matrix of zeroes and ones relating the present and future states. This is called the T matrix representation of the network. If X is the initial state then the sequence of states through which the shift register will pass during successive times is given by

$$X,\ TX,\ T^2X,\ T^3X\ \ldots$$

The sequential properties are derived from the algebraic properties of T. The inverse of T matrix, T^{-1} can be interpreted as the operation that takes the network from a given state to the state that immediately preceded

it in time. If T^{-1} exists and unique for each possible state there is a unique predecessor, and the network is called non-singular. A matrix T has a unique inverse if and only if its determinant is not zero. In the above example ·

$$T^{-1} = \begin{bmatrix} 0 & 1 & 0 \\ 0 & 0 & 1 \\ 1 & 0 & 1 \end{bmatrix} \text{ and } |T| = 1 \qquad (4\text{-}4)$$

The sequential behaviour of a network may be represented by a state diagram where the nodes represent the states of the network and arrows joining the nodes represent the allowed transitions. The number of nodes in the state diagram for a mod-p-network with n delay elements (Flip flops in binary) will be p^n. For deterministic networks where the present state uniquely determines the next state, exactly one arrow leaves each node. For deterministic and nonsingular networks each node will have exactly one arrow leaving and one arrow entering it. Applications of network equations (4-1) yeild the state diagram shown in Fig. 4-2.

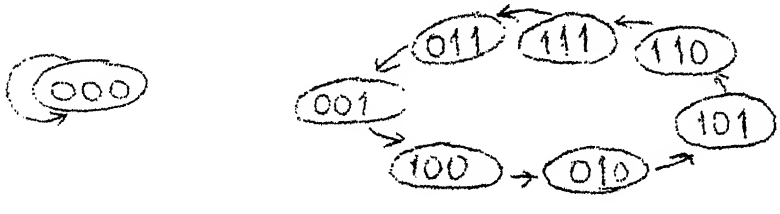


Fig. 4-2.

It consists of 1 cycle and 7 cycle. The one cycle is the trivial one, from the initial state (000) which goes into itself for linear network. All the remaining $2^3-1=7$ states form a single cycle. This indicates that the network is a maximal cycle network. The fact that the network is a maximal cycle network can be found by considering the chracteristic polynomial without considering the state diagrams. The characteristic polynomial of the T matrix is

$$\varphi(x) = |T - x I| \qquad \text{where I is the Identity matrix.}$$

In the above example it is

$$\varphi(x) = \begin{vmatrix} -x & 1 & 1 \\ 1 & -x & 0 \\ 0 & +1 & -x \end{vmatrix} = x^3 + x + 1 \qquad (4\text{-}5)$$

The coefficients are reduced to moduls 2 arithmetic

$$\varphi(0) = |T| = 1$$

A square matrix satisfies its own characteristic polynomial equation. Thus

$$\varphi(T) = T^3 + T + I = 0 \qquad \ldots. \quad (4\text{-}6)$$

The matrix period is the smallest integer k for which $T^k = I$. Thus $T^k X = X$ for any initial state X. k is found from the characteristic equation.

From eqn.4-6 $T^3 = T + I$

$$T^3 \cdot T^3 \cdot T = (T+I)^2 T = (T^2 + I)T = T^3 + T = I$$

Hence $T^7 = I$

To find matrix period itis sufficient to find an integer k such that the polynomial $\varphi(x)$ divides $x^k - 1$ without remainder

If $x^k - 1 = \varphi(x)\ q\ (x)$

we have $T^k - I = \varphi(T)\ q\ (T) = 0$

so that $T^k = I$

The smallest such integer then determines the period. In our example we find $x^7 - 1 = (x^3 + x + 1)(x^3 + x^2 + 1)(x - 1)$. The above factors of $x^7 - 1$ are irreducible i.e. prime factors.

Maximal period network: A maximal period linear sequential network with n delay elements is one for which the state diagram consists of one cycle of length $p^n - 1$ plus the trivial cycle. It has been shown by Zierler[3] that a necessary condition for a binary linear feedback shift register to

have maximal period is that the characteristic polynomial be irreducible.

The necessary and sufficient condition for maximality is that $\varphi(x)$ be irreducible and that it not be a divisor of x^k-1 for any integer $k < p^n-1$.

The generating polynomial $g(x)$ is defined as the ideals generated by $g(x)$ in the algebra of polynomials modulo x^k-1, as $(x^k-1)/\varphi(x)$, whose coefficients (0 or 1) are the sequence bits.

Table I shows all the binary irreducible polynomials through n = 5 along with the corresponding periods.

Table I

Binary Polynomials

Coefficient of x^0	x^1	x^2	x^3	x^4	x^5	Period	Feedback Coefficients
0	1					Singular	0
1	1					1	1
1	1	1				3	1 1
1	1	0	1			7	0 1 1
1	0	1	1			7	1 0 1
1	1	1	1	1		5	1 1 1 1
1	1	0	0	1		15	0 0 1 1
1	0	0	1	1		15	1 0 0 1
1	0	1	0	0	1	31	0 0 1 0 1
1	0	0	1	0	1	31	0 1 0 0 1
1	1	0	1	1	1	31	1 1 0 1 1
1	1	1	0	1	1	31	1 0 1 1 1
1	0	1	1	1	1	31	1 1 1 0 1
1	1	1	1	0	1	31	0 1 1 1 1

The feedback logic for maximum length sequence is given upto 20 stages in Table II.

Table II

No.of stages m	Feedback logic	No.of stages m	Feedback Logic
1.	$X_n = X_{n-1}$	11.	$x_n = x_{n-9} \oplus x_{n-11}$
2.	$x_n = x_{n-1} \oplus x_n{}^{-2}$	12.	$x_n = x_{n-2} \oplus x_{n-10} \oplus x_{n-11} \oplus x_{n-12}$
3.	$x_n = x_{n-2} \oplus x_{n-3}$	13.	$x_{n-1} \oplus x_{n-11} \oplus x_{n-12} \oplus x_{n-13}$
4.	$x_n = x_{n-3} \oplus x_{n-4}$	14.	$x_n = x_{n-2} \oplus x_{n-12} \oplus x_{n-13} \oplus x_{n-14}$
5.	$x_n = x_{n-3} \oplus x_{n-5}$	15.	$x_n = x_{n-14} \oplus x_{n-15}$
6.	$x_n = x_{n-5} \oplus x_{n-6}$	16.	$x_n = x_{n-11} + x_{n-13} + x_{n-14} + x_{n-16}$
7.	$x_n = x_{n-6} \oplus x_{n-7}$	17.	$x_n = x_{n-14} \oplus x_{n-17}$
8.	$x_n = x_{n-2} \oplus x_{n-3} \oplus x_{n-4} \oplus x_{n-8}$	18.	$x_n = x_{n-11} \oplus x_{n-18}$
9.	$x_n = x_{n-5} \oplus x_{n-9}$	19.	$x_n = x_{n-14} \oplus x_{n-17} \oplus x_{n-18} \oplus x_{n-19}$
10.	$x_n = x_{n-7} \oplus x_{n-10}$	20.	$x_n = x_{n-17} \oplus x_{n-20}$

4-2 Properties of PN sequences: Maximum length shift register sequences have the following randomness properties.

4-2-1. Balance property: In each period of the sequence the number of ONE'S and ZEROE'S differ by atmost 1.

4-2-2. Run property: Among the runs of ONE'S and zero's in each period one half the runs of each kind are of length one, one fourth of each kind are of length two, one eighth are of length three and so on.

4-2-3. Correlation property: If a period of sequence is compared bit by bit with any cyclic shift of itself the number of agreements differ from the number of disagreements by at most 1.

The PN sequences are important because of their correlation properties. The normalised correlation of such a sequence is defined as

$$\rho(\tau) = \frac{A - D}{A + D}$$

Where A is no. of agreements

D is no. of disagreements

τ is no. of cyclic shifts.

At zero time lag i.e. for $\tau = 0$ the peak value of ρ is 1 for all other values of τ, it is $-\frac{1}{2^m - 1}$. This property is analogous to the correlation property of the white noise. The sequence is nearly orthogonal to the cyclic shift of itself. When the no. of stages is very large, a moderately long segment of the sequence will exhibit the same auto-correlation property.

4-3 Hardware Design: The period of PN sequence must be at least as great as the multipath duration. If it is less, paths of seperation equal to a period or its multiple will be indistinguishable. Secondly the autocorrelation peak value ($2^n - 1$) must be very much larger than its minimum value, - 1. A 15 stage shift register sequence will have a maximum sequence length of $2^{15} - 1$, (32,767 bits) and at 10 MHz clock rate the period is 3.2767 m sec. The feedback logic is the mod-2 sum of 14^{th} and 15^{th} stage output fed back to the first stage. (See Table 4-2). An adequate period of 3.2767 m sec., desirable autocorrelation levels and simple feedback logic favour the choice of 15 stages for the PN sequence generator.

We have already seen in Sec. 4-1 that the circuit remains in the trivial state (zero state) if all the shift register outputs are'0'. To avoid such a situation we commence the sequence from a reference state of all '1's, We use a Schmitt trigger, and a 2- input OR gate along with the EXCLUSIVE OR to achieve this.

The EXCLUSIVE OR gate output is connected to one of the OR gate inputs. The second input to the OR gate may be connected either to '1' (+ 5V) or '0' (ground) . The initial state of all'1' 's can be achieved by giving'1' input to the OR gate. when 15 clock pulses are given all

the shift registers store '1'. Now if the OR gate input is made zero, the output of the OR gate is the same as EXCLUSIVE OR gate and the generator gives out PN sequence. A switch which is connected either to + 5V or ground can give '1' or '0' input to the OR gate. Because of contact bounds the transitions from '1' to'0' will not be fast. A schmitt trigger with fast transition is desirable under such circumstances. The schematic is given in Fig. 4-3. The shifted version of the PN sequence is available at each of the Q outputs of flipflops.

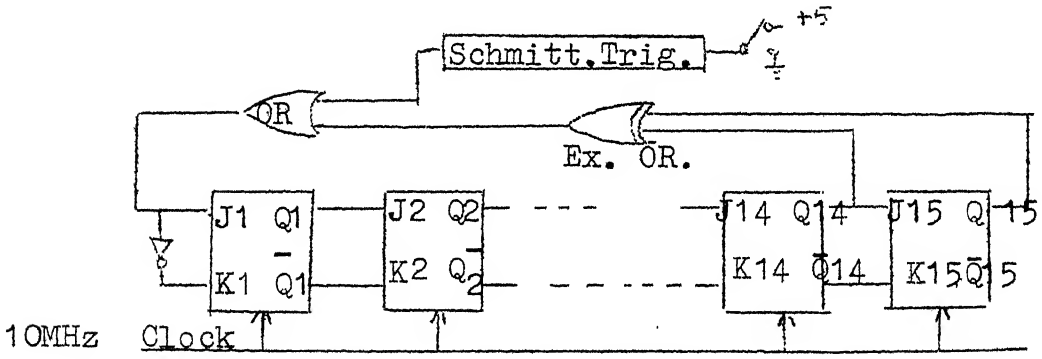


Fig. 4-3. 15 stage feedback shift register for generating PN sequence.

EXCLUSIVE OR gate: The realisation of 2-input EXCLUSIVE OR Logic using 4- NAND gates is given in Fig. 4-4.

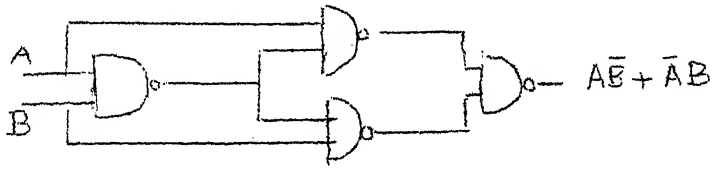


Fig. 4-4. Exclusive OR Gate.

" OR " gate and Schmitt Trigger:- Four 2-input NOR gates are used as in Fig. 4-5 for the OR gate and Schmitt trigger.

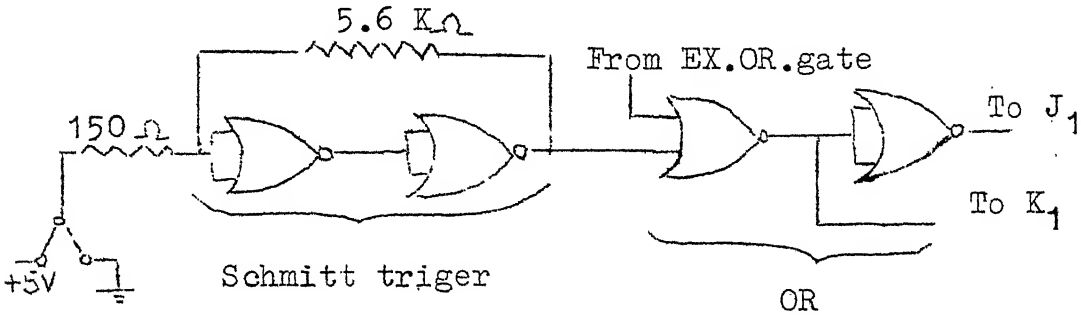


Fig. 4-5 Schmitt Trigger and OR gate.

When the Schmitt trigger input terminal is connected to + 5V supply the output of Schmitt trigger is at '1' level. Hence the OR gate output is '1' whatever the output of Ex-OR gate and the shift registers store '1' in 15 clock duration. The input of Schmitt trigger is grounded after 15 clock duration. The Schmitt trigger output now is '0' and the output of OR gate is the same as the output of EX-OR gate. Hence the generator gives out PN sequence. A push button switch is used at the input of the Schmitt trigger to connect it to either +5V or ground.

To synchronise two such generators the schmitt trigger output of one generator must be given to the OR gate input of the second one.

4-4. Testing: Since the length of the sequence is $2^{15}-1 = 32.767$, at 10 MHz clock rate it is difficult to obtain a steady pattern on the oscilloscope, for checking the sequence. To ensure proper functioning of the PN sequence generator, two tests are done.

4-4-1. Test I. Maintaining a clock width of 50 ns. (corresponding to the width at 10 MHz rate), clock pulses are given manually. The schmitt trigger input is connected to + 5V initially, to store '1' s in all the shift registers. It is then connected to ground . After each clock pulse input the output of the first flip flop Q_1 is noted. The output is checkedbit by bit upto about 650 bits. It is seen that the output ~~floows~~ follows the expected pattern.

4-4-2. Test 2: In this test only the 1st and the 15th flip flop are taken into account. The test circuit is as shown in Fig. 4-6. This test is mainly to ensure that there is no logic hazard due to propagational delay.

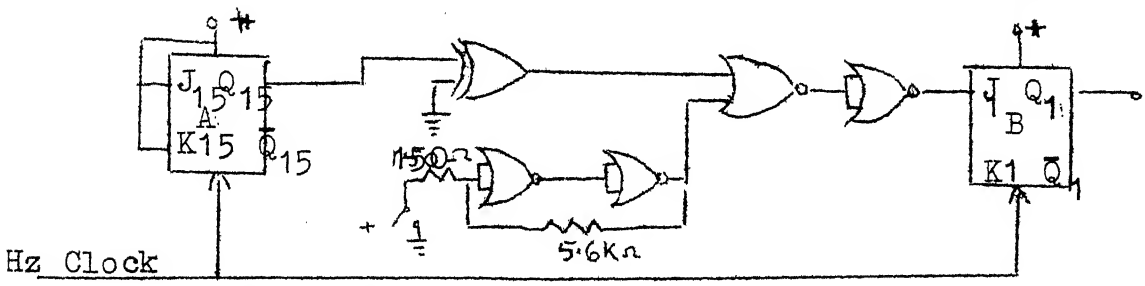


Fig. 4-6. Schematic For Test 2.

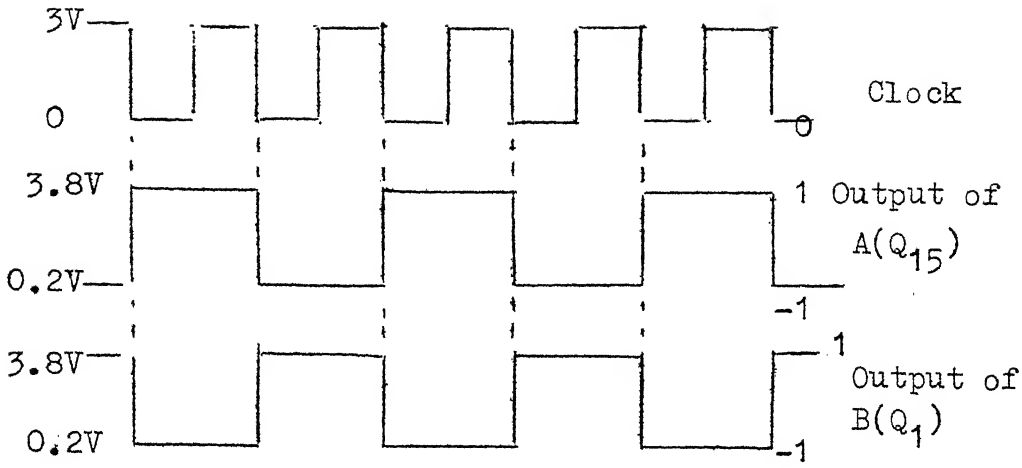


Fig. 4-7 Schematic For Test 2.

The flip flop A is a toggle. Output of flipflop A changes its level for each clock pulse. The output of flipflop B remains at 1 when Schmitt Trigger output is 1. With Schmitt trigger output at zero, whenever the clock pulse is given the input to B appears as output of B. In otherwords B is connected as D type flipflop which gives unit delay. The logic block in betweengives the same propagation delay, as in the feedback of the PN sequence generator. The observed wave forms are givenin Fig. 4-7.

The two test results together ensure proper functioning of the PN sequence generator.

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1. Elspas: "The Theory of Autonomous Linear Sequential Networks" IRE transactions on Circuit Theory pp 45-60 March 1959.

2. Edt. by S.W. Goulomb; " Digital Communication with Space Applications", Prentice Hall. Englewood Cliffs N.J. 1964.

3. Neal Zierler: " Linear Recurring Sequences" , Journal of the Society for Industrial and Applied Mathematics pp 31-47 Vol. 7 Number 1, March 1959.

4. Edt. By Robert. L. Morris And Rohn. R.Miller: "Designing with TTL Integrated Circuits", Texas Instruments Electronics Series Mcgraw Hill.

CHAPTER V

CORRELATOR

The system description, working and Hardware design of correlator are presented here.

5-1. System Description: At the Rake taps of the receiver, the inphase and quadrature components of received signal w(t) is cross correlated with the τ_i shifted version of the PN sequence using current switch. Mathematically cross correlation of two periodic signals x (t) and y(t) is equivalent to the product of the two signals, with one of them delayed, which is then averaged over the period, with delay as the running variable, as given in eqn. (5-1)

$$R_{xy}(\tau) = \frac{1}{T}\int_{t}^{t+T} x(t)\, y(t+\tau)\, dt \quad \ldots \quad 5\text{-}1$$

where T is the period of x(t) and y(t) .

The block diagram representing the correlator is shown in Fig. 5-1.

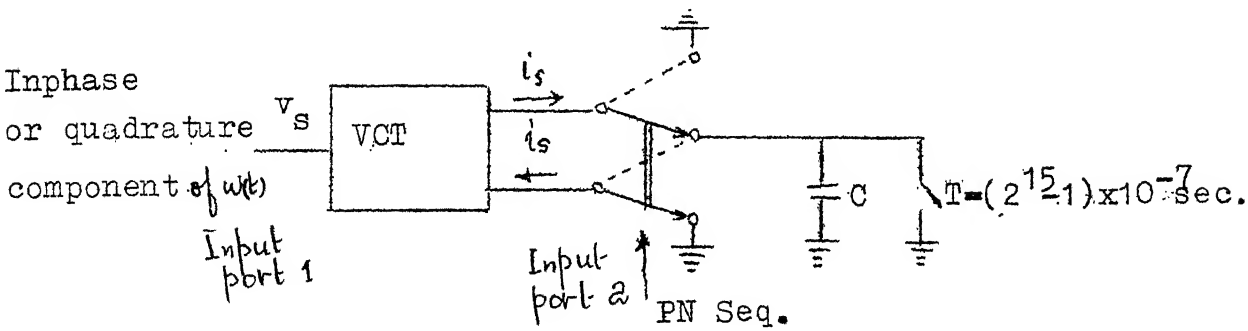


Fig. 5-1. Block diagram of correlator.

In our case the multiplier is the PN sequence having binary voltage levels corresponding to + 1 and -1. Hence multiplication can be easily achieved, by a balanced current, proportional to the multiplicant, namely the signal voltage, as shown in the Fig. 5-1. Integration is performed by passing the current through a capacitor and by measuring the voltage developed across its terminals.

The switch position is decided by the PN sequence level, when the PN sequence level is '1' a current 'i_s' proportional to the signal voltage v_s charges the capacitor C. when the PN sequence level is '-1' the current 'i_s' proportional to v_s , discharges the capacitor C. At the end of one sequence period (3.2767 m sec.) the capacitor voltage is sampled and reset to an initial voltage condition.

Thus we must obtain equal and opposite currents proportional to v_s and a switch, switched by PN sequence.

5-2. Voltage to current Transuder (VCT): As the name indicates the output current of the VCT is proportional to the input voltage v_s . Consider the circuit in Fig. 5-2.

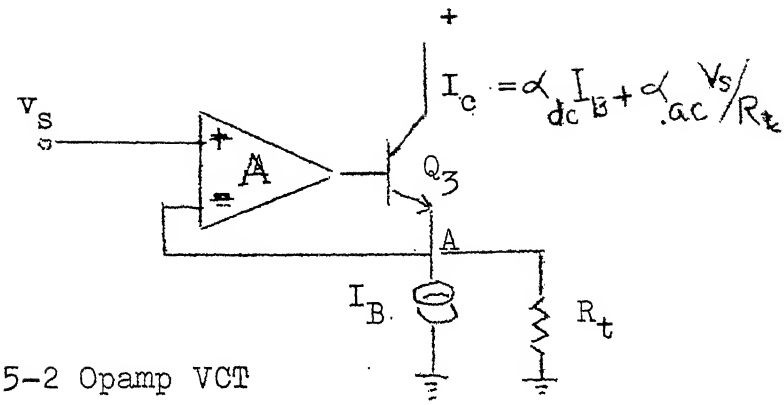


Fig. 5-2 Opamp VCT

The voltage v_s is applied to a high gain (A) amplifier, with a transistor in the feedback configuration. We see that the voltage at the node A is equal to the input voltage, if A tends to infinity. The current sink provides the bias current, I_B, for the transistor Q_3 (neglecting the input bias current of the amplifier). If a resistance R_t is connected between node A and ground a current flows through R_t . Hence the collector current of the transistor Q_3 is $I_c = \alpha_{dc} I_B + \alpha_{ac} v_s / R_t$ .... 5-2. Thus the transconductance of the VCT will be

$$\alpha_{ac} / R_t \qquad \ldots\ldots\ldots \qquad 5\text{-}3.$$

Because of the bandwidth considerations an opamp of the type μA 741 cannot be used in the circuit given in Fig. 5-2. Hence a simple finite gain differential-amplifier (diff amp) is used as shown in Fig. 5-3.

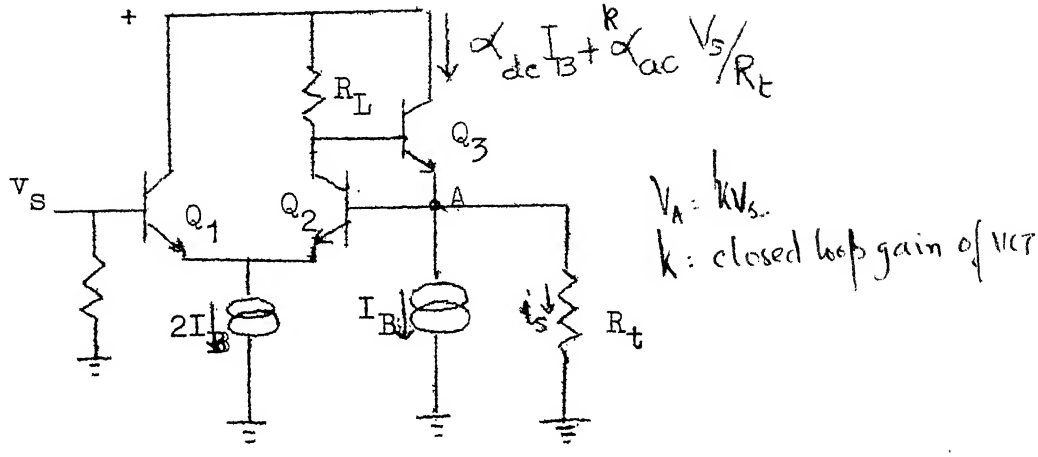


Fig. 5-3 Diffamp. VCT

The transconductance and bandwidth considerations of the VCT using a finite gain amplifier are given in Appendix.

5-3. Voltage to current Transducer with a balanced current output:- A differential voltage to current transducer (DVCT) is obtained by interconnecting two single ended circuits as shown in Fig. 5-4. The resistance R_t is now connected tothe second VCT as shown. When the inputs v_s and v_s' are zero the potential at the nodes A and B are ~~nominally~~ virtually at zero volts and no current flows through R_t. The collector currents of Q_3 and Q_4 are now $\alpha_{dc} I_B$. With v_s' zero, node B will be at virtual ground. When v_s is applied, a signal component of current $i_s = kv_s / R_t$ flows

The potential at node A is kv_s and

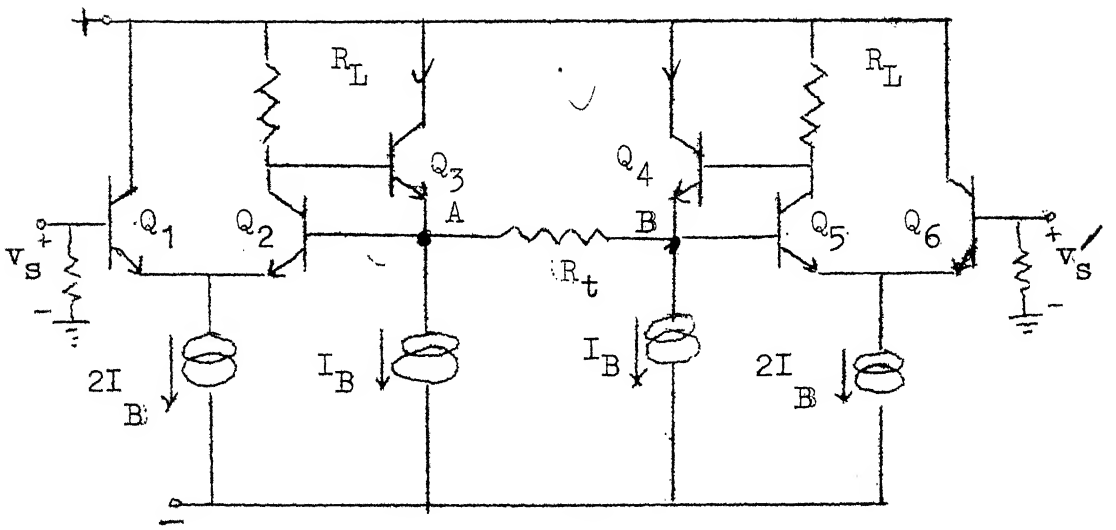


Fig. 5-4: VCT with a balanced current output.

through R_t. Applying KCL at nodes A and B, if the base currents of Q_2 and Q_5 are neglected, we see that the collector current of Q_3 is $\alpha_{dc} I_B + \alpha_{ac} k v_s/R_t$ and that of Q_4 is $\alpha_{dc} I_B - \alpha_{ac} k v_s/R_t$. It is thus possible to get balanced current outputs proportional to signal. The transconductance is decided by R_t and is approximately equal to $k\alpha_{ac}/R_t$.

5-4. Current switch: Equal and oposite current outputs generated by the DVCT are to be switched by the PN sequence. Speed and coupling considerations make one choose the emitter coupled configuration, shown in Fig. 5-5.

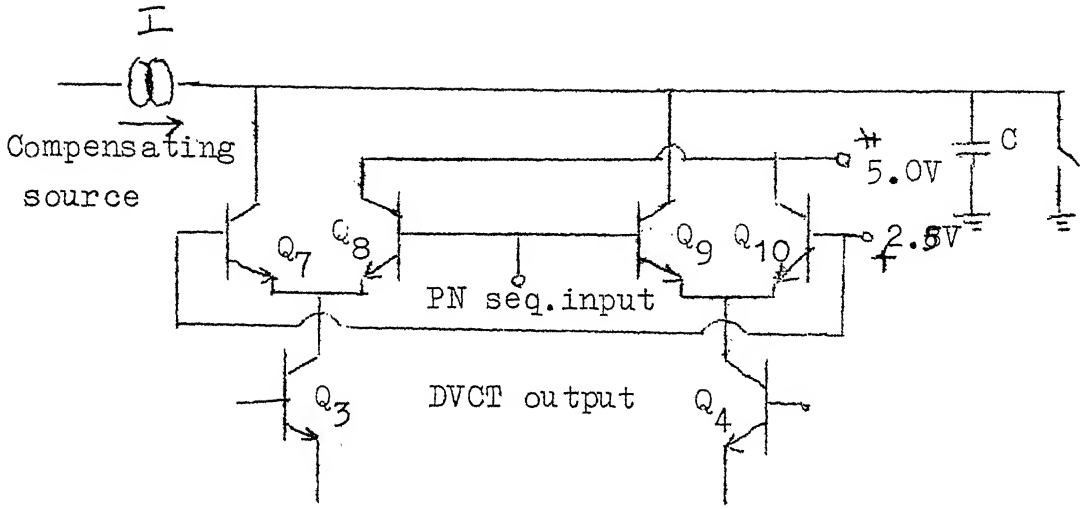


Fig. 5-5 Current Switch.

The bases of Q_7 and Q_{10} are connected to a voltage +2.5v so that Q_3 and Q_4 (of the DVCT circuit) are biased properly. PN sequence levels are modified as 2.1V (-1 level) and 3.5v (+ 1 level). These are applied to the bases of the transistors Q_8 and Q_9 . The collectors of Q_7 and Q_9 are connected together and a current source is provided as shown which cancells the dc bias current $\alpha_{dc} I_B$ of the DVCT, which also gets switched. Transistors Q_8 and Q_9 conduct when the PN sequence level is '+1'. Under these conditions a current $\propto \left[\alpha_{dc} I_B + \alpha_{ac} k V_s / R_t\right]$ flows through the collector of Q_8 and a current $\propto \left[\alpha_{dc} I_B - \alpha_{ac} k V_s/R_t\right]$ flows through the collector of the transistor Q_9 . (α is the common base shortcircuit current gain of Q_8 and Q_9). A constant current source is provided as shown which cancells the d-c bias current $\propto \alpha_{dc} I_B$ and the net signal current charges

the capacitor C. When the PN sequence level is '1' Q_8 and Q_9 are off and Q_7 and Q_{10} are on $\alpha\left[\alpha_{dc} I_B - \alpha_{ac} k v_s / R_t\right]$ flows in the collector of Q_{10} and a current $\alpha\left[\alpha_{dc} I_B + \alpha_{ac} k v_s / R_t\right]$ flows in the collector of Q_7. Once again the current which discharges the capacitor is equal to signal component $-\alpha\alpha_{ac} k v_s / R_t$.

Since this current is switched at 10MHz, an opamp can not be used for integrating (see Sec.2. appendix).

Considering only the integrator part we can represent it by its equivalent circuit as shown in Fig. 5-6. R_o is the equivalent output resistance of the two current sources, whose magnitude depends on the devices employed. Thus for a finite value of R_o we will have a pseudo-integrator (low pass filter). The time constant R_oC decides the cut off frequency of the filter and the circuit behaves as an ideal integrator for frequencies very much greater than $1/2\pi R_oC$.

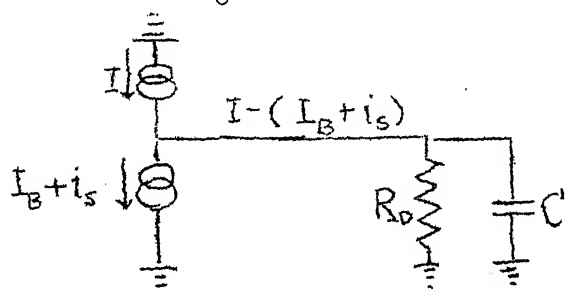


Fig. 5-6

Under quiscent conditions ($i_s = o$) , if the compensating current is not exactly equal to the bias current, $\alpha\alpha_{dc} I_B$ of the transistor, the difference current through R_o gives rise to an output d-c voltage ($I - \alpha\alpha_{dc} I_B$) $R_o = I_d R_o$. If the difference current I_d is considerable , the output voltage will result in a latch up condition, where the transistors operate in saturation mode. Since the difference current I_d will be slowly varying with changes in ambient temperature, power supply voltage etc, this results in a drift at the integrator output. To keep this drift voltage within 1% of the dynamic range of the output voltage (V_D) , the allowable magnitude of the difference current I_d should be

$$I_d = \frac{0.01\ V_D}{R_o}$$

Assuming a dynamic range of 1V for the output and taking a typical value of 100 K for R_o, I_d must be within 0.1 μA. Practically it is impossible to obtain such a close matching between I and $\alpha\alpha_{dc} I_B$, over a wide temperature range. The situation can be improved by providing the feedback arrangement shown in Fig.5-7. The functions of the feedback is to maintain the d.c. level at the output, at a particular value (5 volts, chosen for proper biasing of transistors). Any change

in the output d.c. level is compared with a fixed reference voltage (5 volts). The difference is amplified and passed through a low pass filter. The output of the filter is fed to the compensating current source as shown in Fig. 5-7.

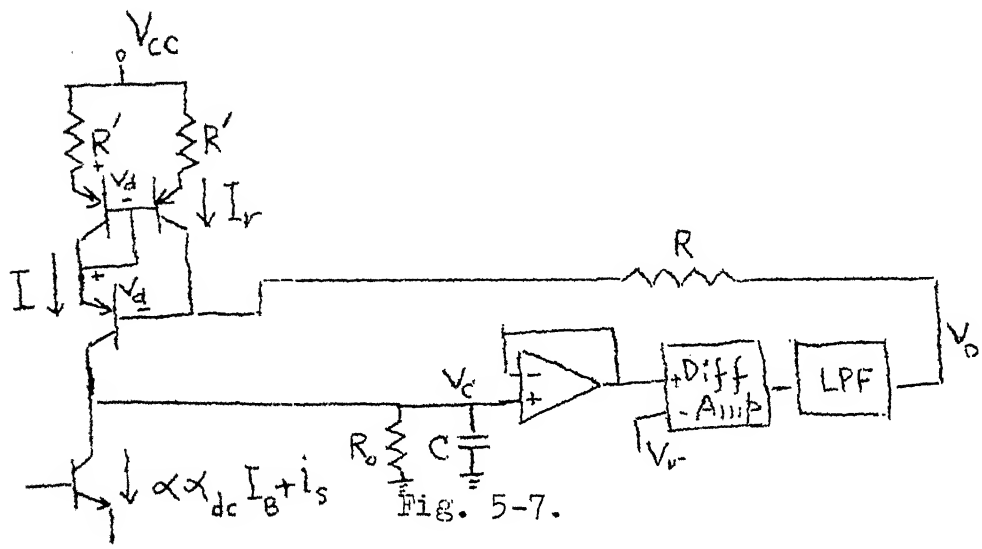


Fig. 5-7.

The compensating current source is designed using pnp transistors arranged in a configuration due to Wilson (see appendix) . This arrangement provides a unity gain current controlled current source (CCS) of high output resistance and excellent linearity. The reference current I_r which forms the input into the CCS is given by

$$I_r = \frac{V_{cc} - 2V_d - V_o}{(R + R')}$$

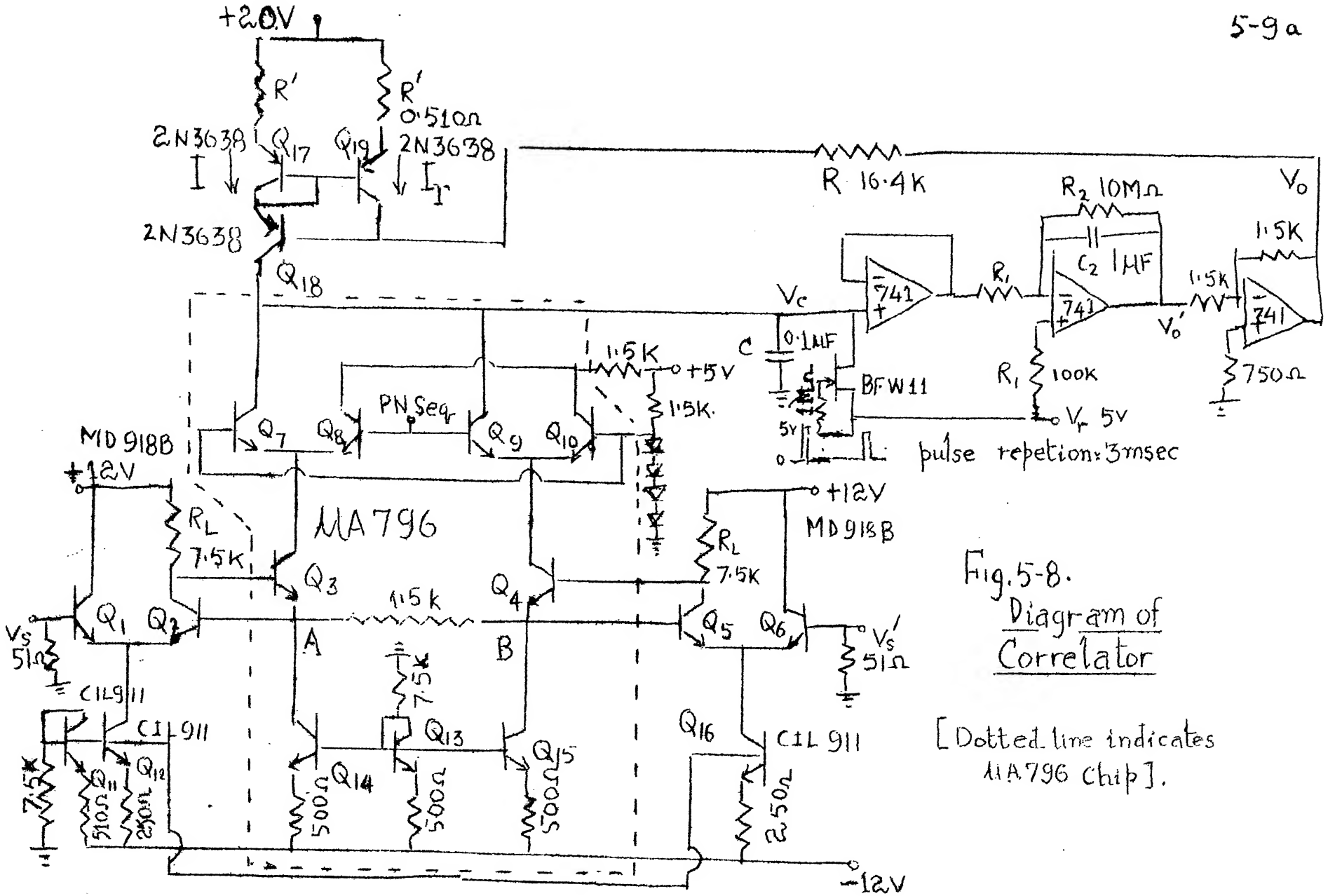


Fig. 5-8. Diagram of Correlator

[Dotted line indicates µA796 chip].

It can be easily seen that if the capacitor voltage V_c tends to rise, V_o also rises and I_r is reduced, which in turn reduces I so that the output d.c. is maintained at the reference value. The low pass filter is designed to have a cut off frequency much lower than that of the pseudointegrator, so that the integrated signal frequency components appearing at the output are attenuated. In other words, the negative feedback loop operates only for the drift components in the circuit.

Consider the s domain relationship between the signal current I_s and the integrated output voltage V_c given by (Fig 5-7A)

$$V_c = I_s Z(s)$$

where Z(s) is the transfer impedance function. Considering only the ac components, the voltage developed across C is given by (Fig. 5-7 A)

$$V_c = (I_r - I_s)\frac{R_o}{(s CR_o + 1)} = \frac{(I_r - I_s)}{c(s + 1/CR_o)} \quad \ldots\ldots \quad (5\text{-}5)$$

But $I_r = -\frac{V_o}{R}$, substituting in (5-5) we get

$$V_c = \left(-\frac{V_o}{R} - I_s\right)\frac{1}{C(s + 1/CR_o)} \quad \ldots\ldots \quad (5\text{-}6)$$

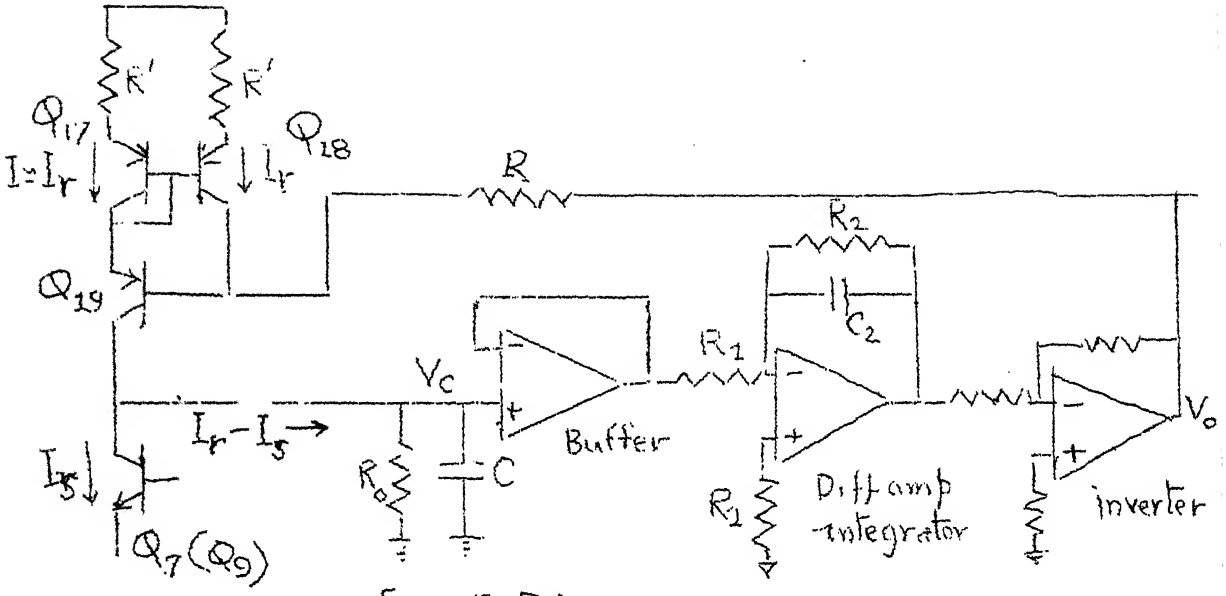


Fig. 5-7A.

The diffamp and lowpass filter output after inversion is given by $V_o = \frac{V_c}{R_1 C_2} \times \frac{1}{(s + 1/C_2 R_2)}$ .... (5-7)

Substituting for V_o in 5-6

$$V_c = - \frac{1}{RC\left(s + 1/CR_o\right)} \times \frac{V_c}{R_1 C_2 (s + 1/R_2 C_2)} - \frac{I_s}{C(s + 1/CR_o)}$$

After simplication we get,

$$\frac{V_c}{I_s} = - \frac{1}{C} \times \frac{(s + 1/R_2 C_2)}{\left[(s + 1/CR_o)(s + 1/R_2 C_2) + \frac{1}{R_1 C_2 RC}\right]} \quad ..(5-$$

This can also be written in the form

$$\frac{V_c}{I_s} = - \frac{(s + 1/R_2 C_2)}{C\left[s^2 + s(1/R_2 C_2 + 1/CR_o) + (1/R_1 C_2 RC + 1/R_2 C_2 CR_o)\right]} \quad ...(5-9)$$

$$\frac{V_c}{I_s} = - \frac{(1 + 1/s\tau_2)}{Cs\left[1 + (1/s\tau_2 + 1/s\tau_o) + (1/s^2\tau_3\tau_4 + 1/s^2\tau_2\tau_o)\right]} \quad \ldots (5\text{-}10)$$

where $\tau_2 = R_2 C_2$, $\tau_o = R_o C$, $\tau_3 = R_1 C_2$, $\tau_4 = RC$

We see that as s takes large values, the transfer impedance approaches that of ideal integrator.

From 5-9 we see that thepeak value of Z(s) occurs at $w_p = \sqrt{1/R_1 C_2 RC + 1/R_2 C_2 CR_o}$ rad/sec..(5-11)

w_p can be brought down by increasing C_2 and R_1.

The entire circuit of correlator is given in Fig. 5-8.

5-5. Design: Current sink: - Referring to Fig. 5-8 Q_{11}, Q_{12}, Q_{13}, Q_{14}, Q_{15}, and Q_{16} constitute the current sinks which provide the biasing currents to Q_1, Q_2, Q_3, Q_4, Q_5, and Q_6.

The biasing current I_B is given by (see appendix)

$$I_B = I_r = \frac{V_{cc} - V_d}{R_B + R_1'}$$

$$R_1' = 510\,\Omega$$

Choosing $V_{cc} = \pm 12$V and $R_B = 7.5$K, I_B is 1.45 mA.

When the inputs to the DVCT are grounded, nodes A and B must be at virtual ground. Therefore, under quiscent conditions, the base voltage of Q_3 (Q_4) and collector voltage of Q_2 (Q_5) must be 0.7V. R_L is chosen such that $V_{cc} - I_B R_L = 0.7V$.

With V_{cc} = + 12V, I_B = 1.45 mA $R_L \simeq$ 7.5 K.

The bases of Q_7 and Q_{10} are maintained at $\simeq$ 2.5V. Therefore, the collector potential of Q_3 (Q_4) $\simeq$ 1.8V. If the input signal is within 1.8V the collector base junction of Q_3 and Q_4 will be reverse biased.

Compensating Current Source: A supply voltage of 20V. is chosen, to have a good dynamic range of the output voltage V_c. Under quiscent conditions, with V_o zero (Low pass filter output), R is chosen such that

$$I = \alpha\alpha_d I_B \simeq 1.45 \text{ mA} \times 0.96,$$

$$I = I_r = \frac{V_{cc} - 2 V_d}{R + R_1'} \quad \text{(see appendix)}$$

$R_1' = 510$, R = 16.2K is chosen.

Low Pass Filter design: The differential amplifier integrator shown in Fig. 5.9, attenuates the signal frequency component of V_c. The output voltage V_o' of filter is

$$V_o' = V_r - \frac{(V_c - V_r) R_2}{R_1 (sC_2R_2 + 1)}$$

$$V_o' = V_r \left(1 + \frac{R_2/R_1}{sC_2R_2+1}\right) - \frac{V_c R_2/R_1}{sC_2R_2+1}$$

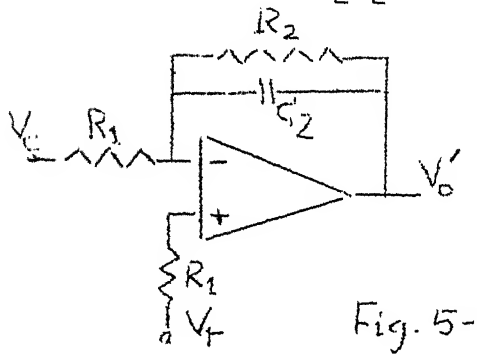


Fig. 5-9.

A d.c. gain of 100 is obtained by choosing R_1= 100 KΩ and R_2 = 10MΩ.

With C_2= 1 μF, the cut off frequency is $\frac{1}{A_o C_2 R_1}$ = 0.1 rad/sec.

5-6 Testing:

5-6-1: Pulse Response: For a periodic pulse at 10 MHz the response at node A (VCT output) is observed. The input pulse level is 1 V and rise time is 1 ns. The output voltage at node A is 1 V with rise and falltimes 10 ns.

5-6-2: D.C. voltages from -1.5V to + 1.5V in steps of 0.1V is applied and the DVCT output at node A is observed. The closed loop gain variation is from 0.96 to 0.99. The output saturates above 1.53V.

5-6-3: Symmetrical square wave of amplitude ± 1 V is applied at the input port 1. (signal port). The input port 2 (PN sequence) is kept at +'1' level and waveform at the correlator output is observed.(Fig. 5-10-(b)) . With the input port 2 at -'1' level the output wave form is seen inverted .(Fig. 5-10(c)). The wave forms are observed from 1Hz onwards. Above 25 Hz linearity is observed.

5-6-4: Frequency response of correlator: With input port '2' kept at +'1' level the correlator output is observed for sinewave inputs with frequencies from 1Hz to 10 MHz. The magnitude plot V_c/V_s is given in Figure 5-11 for two values of R_1 (10K and 100K). For the values chosen , the frequency

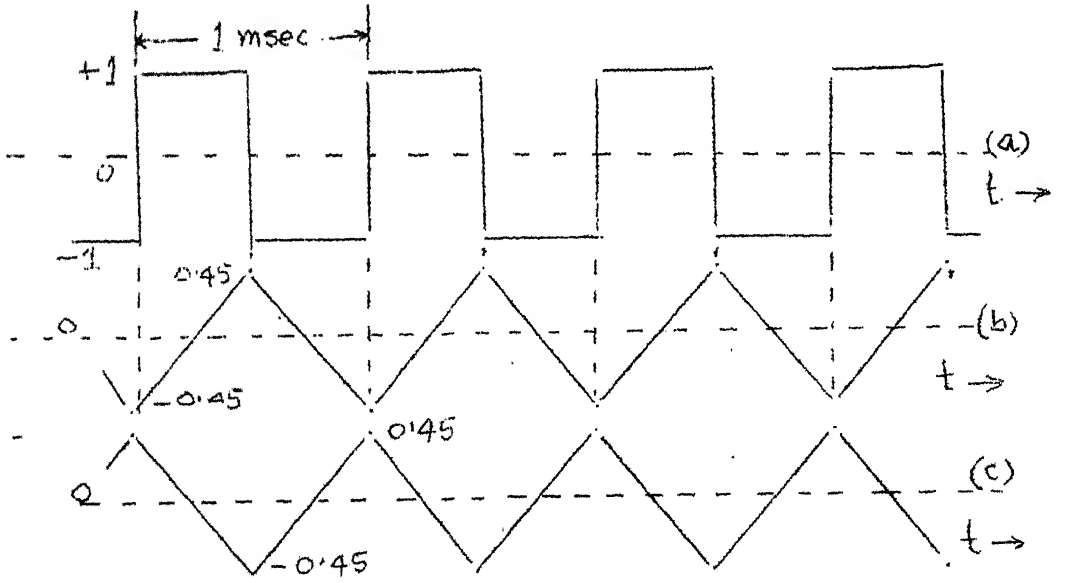


Fig. 5-10(a) Squarewave input (b) output when the PN sequence input port is kept at +'1' level (c) output when PN seq. input port is kept at -'1' level.

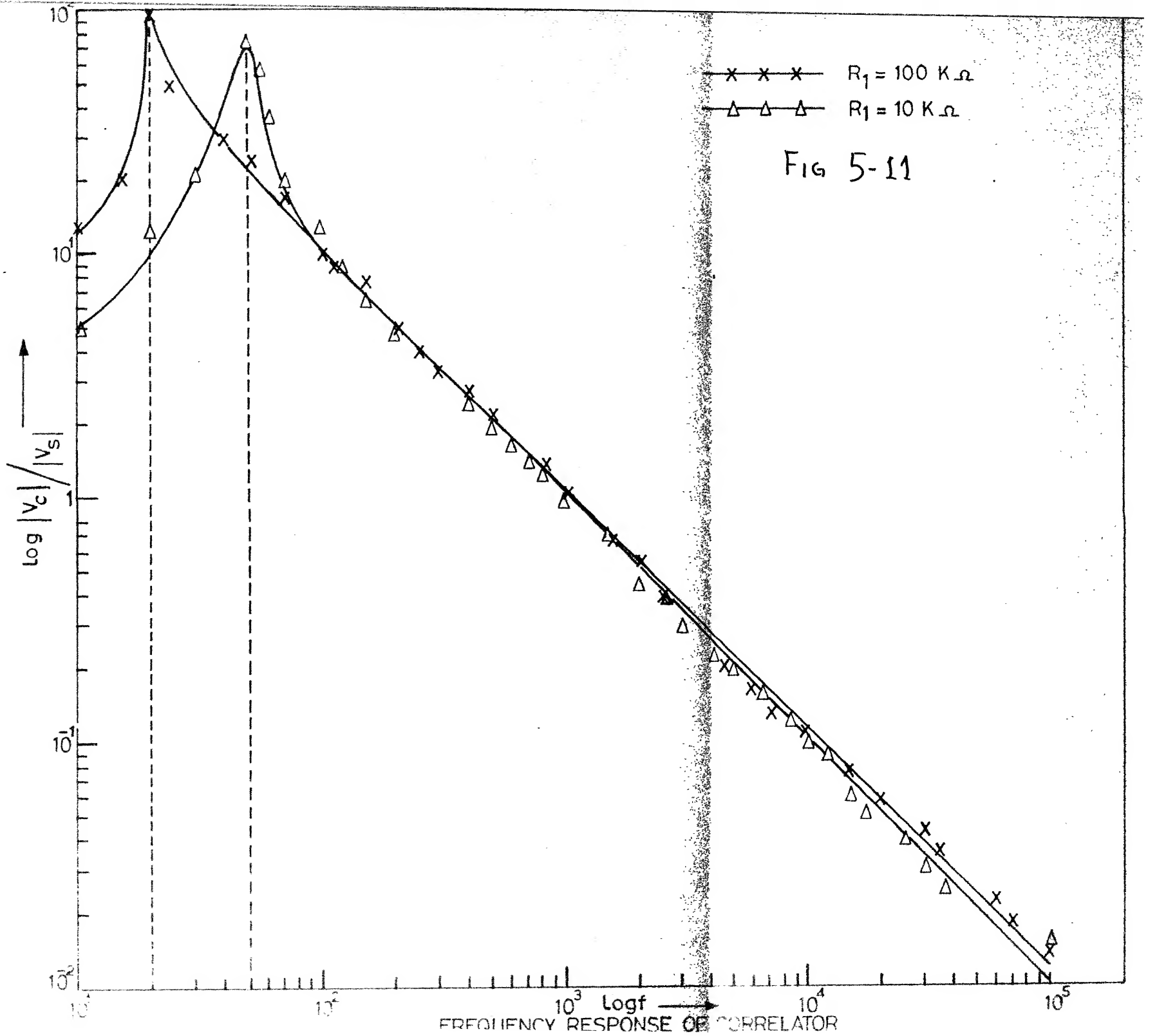


FIG 5-11

FREQUENCY RESPONSE OF CORRELATOR

w_p, at which the peak occurs satisfies eqn. 5-11. When R_1 = 100K , above 25 Hz the response is similar to that of anideal integrator. When R_1 = 10K, above 70 Hz the response is similar to that of an ideal integrator.

Reference:

1. George R. Wilson " A monolithic Junction FET npn Opamp" IEEE Journal of Solid State Circuits Vol. SC3 No.4 Dec. 1968.

APPENDIX 5

5-1. Transconductance and Bandwidth of VCT:

Referring to Fig. 5-3, (Chapter V) the open loop gain of diffamp is $A_o = g_m R_L = \frac{h_{fe}}{1+h_{fe}} \cdot \frac{|I_E|}{\eta V_T} R_L$

with the usual notations.

$$A_o \simeq \frac{|I_E|}{26} R_L \qquad I_E \text{ in mA.}$$

Closed loop gain $= \frac{A_o}{1 + A_o \beta_f}$, where β_f is the feedback factor = 1

With I_E = 1.45mA, R_L = 7.5K, we get A_o = 415 and k, the closed loop gain $= \frac{A_o}{1 + A_o} \simeq 0.99$.

The transconductance of VCT is α_{ac}/R_t

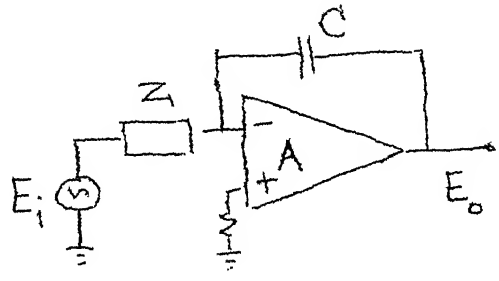
But $\alpha_{ac} = \frac{\alpha_o}{1+j f/f_\alpha} e^{-jm f/f_\alpha}$, m = 0.2 for diffusion transistors.

α_o, is the low frequency value of α (CB short circuit current gain) and f_α is the frequency at which the CB short circuit current gain falls by 3 dB from its low frequency value. $f_\alpha = h_{fe} f_\beta = f_T$ where f_T is the frequency at which the short circuit CE current gain attains unit magnitude.

f_α = 1.2 f_T for diffusion transistors.

Therefore, bandwidth of VCT $\simeq f_T$

5-2: Opamp integrator:



Z: equivalent of source and the input impedance of opamp.

A: open loop gain of opamp.

E_i: input, E_o: output of opamp. ω_o : open loop bandwidth

$E_o = E - \frac{(E_i - E)}{Z} \frac{1}{j\omega C}$, Putting $E = \frac{E_o}{A}$ and

Simplyfying, $\frac{E_o}{E_i} = \frac{1}{\frac{1}{A} + j\omega CZ\left(\frac{1}{A} - 1\right)}$

Putting, $A = \frac{A_o}{1 + j\omega/\omega_o}$ and simplyfing

$$E_o/E_i = \frac{1}{j\omega ZC\left\{\left(1/A_o + j\omega/A_o\omega_o - 1\right) + 1/A_o\, j\omega CZ + 1/A_o\omega_o ZC\right\}}$$

neglecting $1/A_o$, $1/A_o\omega_o ZC$ in the denominator,

$$E_o/E_i = \frac{1}{j\omega ZC\left(\frac{j\omega}{\omega_o A_o}\right) - j\omega ZC}$$

for $\omega \ll \omega_0 A_0$ (gain bandwidth product), $\frac{E_0}{E_i} = -\frac{1/z}{j\omega c}$

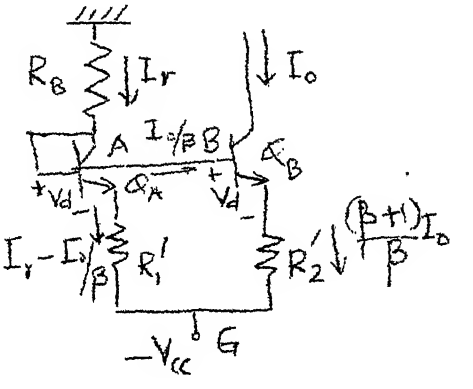
The circuit behaves as an integrator for frequencies for less than the gain bandwidth product $w_0 A_0$.

5-3: Current sink

I_r : Reference current

I_o : Output current

β : Short circuit CE current gain of transistors.



Applying KVL to the loop ABG

$$-(I_r - I_o/\beta)R_1' + (\beta+1)/\beta\, I_o R_2' = 0$$

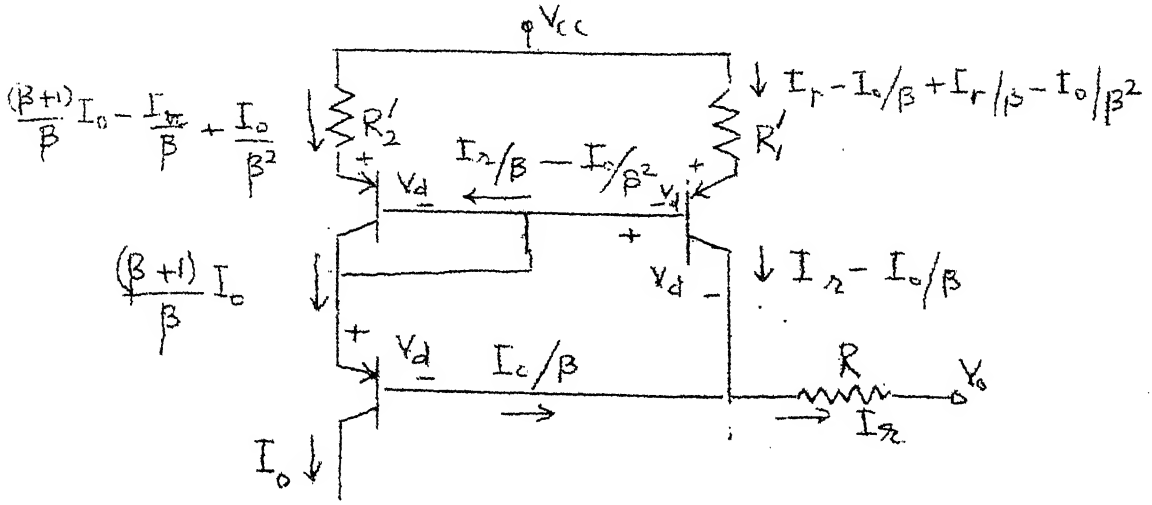
V_{BE} of Q_A and Q_B, are assumed to be equal to V_d.

Simplifying we get, $I_o = I_r R_1'/R_2' \left(1 - \frac{1 + R_1'/R_2'}{\beta + 1 + R_1'/R_2'}\right)$

If $\beta \gg (1 + R_1'/R_2')$ $\quad I_o \simeq I_r R_1'/R_2'$

where I_r is given by $(V_{cc} - V_d)/(R_B + R_1')$.

5-4: Improved current source due to Wilson: (Compensating current source in the Fig. 5-8).



Applying KVL to the lop containing R_1 and R_L and assuming transistors are matched we get,

$$\left[\left(\frac{\beta+1}{\beta}\right) I_o - \frac{I_{r2}}{\beta} + \frac{I_o}{\beta^2}\right] R_2' = \left[I_{r2} - I_o/\beta + I_{r2}/\beta - I_o/\beta^2\right] R_1'$$

Simplifying we get,

$$I_o = I_{r2} \cdot \frac{R_1'}{R_2'} \left[1 + \frac{\beta\left(1+\frac{R_2'}{R_1'}\right) - \beta\left(1+\frac{R_1'}{R_2'}\right) - \left(1+\frac{R_1'}{R_2'}\right)}{\beta^2 + \beta(1+R_1'/R_2') + (1+R_1'/R_2')}\right]$$

for $\beta \gg R_1'/R_2'$, $I_o = I_{r2} \cdot R_1'/R_2'$

when $R_1' = R_2'$, $I_o = I_{r2}\left[1 - \frac{2}{\beta^2+2\beta+2}\right]$

where $I_{r2} = \frac{V_{cc} - 2V_d - V_o}{R + R_1'}$

In the improved current source (i) the errors due to the presence of base current is reduced by a factor of β

(ii) output impedance is increased by a factor of β

(iii) Useful output voltage is increased to βV_{CBO}.

CHAPTER VI

CONCLUSION

The details of the ICs and devices used are given in appendix. For the PN sequence generator the JK master slave flipflops are chosen. However, if D type flipflops are used, the number of connections are reduced. Improved DVCT frequency response was observed when matched pair MD 918B was used for Q_7 - Q_8 and Q_9 - Q_{10}, and 2 N 3572 for Q_3 and Q_4 (Fig. 5-8). The bias currents of Q_3 and Q_4 are tobe matched . Hence a μA 796 IC, where Q_3, Q_4, Q_7, Q_8, Q_9 , Q_{10}, Q_{13}, Q_{14} and Q_{15} are in a single chip, is used.

It is assumed that the signal component of current i_s which charges the capacitor C, has zero average value. This is because the feedback configuration senses the d.c. level appearing at the capacitor output and corrects it. In otherwords $g(t, \xi)$ is assumed to vary very slowly with zero mean value. It is found that the minimum frequency to which the circuit responds is decided by w_p, which in turn depends on ($1/R_1 C_2$ RC + $1/R_2 C_2 R_0 C$) (eqn. (5-11) w_p can be reduced by increasing R_1, C_2, or R_0.

The correlator can also be tested by simulating the tropochannel with about 5 taps, where $g(t,\tau_\ell)$'s are varied using Gaussian noise sources. Samples of $g(t,\tau_\ell)$'s, obtained after correlation, at each of the 5 taps, can be recorded and compared with the record of respective Gaussian noise sources.

Appendix

Pin connections

Pin No.	Card No.1 (PN Seq. Gen.)	Card No. 2 (Correlator)
1	Output Q_2	+ 12V d.c.
2	Q_4	Test point DVCT output node A.
3	Q_6	Test point " " node B.
4	Q_8	V_s' in put to DVCT
5	Q_7	PN seq. input
6	Q_5	Test point Pin 8 of μA 796
7	Q_3	Test point Pin 7 of μA 796.
8	Q_1	-12V dc
9	Q_{15}	Correlator output V_c
10	Q_{13}	Not connected.
11	Q_{11}	Gnd
12	Q_9	Not connected
13	Clock	"
14	Clear (Rd.)	V_s input to DVCT
15	+ 5V dc	Not connected
16	Q_{10}	"
17	Q_{12}	"
18	Q_{14}	"
19	Output of Schmitt trigger	Test point V_o

20	...	Input to Schmitt trigger	...	3 ms pulse input
21	...	Not connected	...	+ 5V d.c.
22	...	Gnd	...	+ 20V d.c.

Device Details

Since the details of the various digital IC's used in the PN sequence generator viz.,

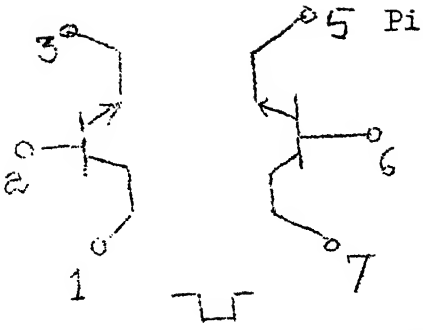
EC 700: Quad 2-input NAND gate used as EXCLUSIVE OR gate.

EC 702: Quad 2-input NOR gate used as OR gate and Schmitt trigger.

EC 773: Dual JK Master Slave Flip-flop used as shift register,

are readily available, they are not given here.

MD 918B: Dual NPN silicon annular transistors designed for ultrahigh frequency differential amplifier applications, requiring a matched pair of transistors with a high degree of parameter uniformity under varying environmental conditions.



Pin connections Bottom view.

Pins 4 and 8 are omitted.

Maximum ratings:

Rating	Symbol	Value	Unit
Collector Emitter Voltage	V_{CEO}	15	V dc
Collector Base Voltage	V_{CB}	30	V dc
Emitter Base Voltage	V_{EB}	5	V dc
Collector current	I_C	50	mA dc

Dynamic characteristics:	Symbol	Min	Max	Unit
Current Gain Bandwidth product (I_c=4mA dc, V_{CE}= 10 V dc, f = 100 MHz)	f_T	600		MHz
Output capacitance				
V_{CB}= 10 V dc, I_E=0, f=140KHz	C_{ob}		1.7	pF
V_{CB}=0 I_E=0 f=140KHz			3.0	
Input capacitance (V_{BE}=0.5V dc, I_C=0, f=140KHz)	C_{ib}		2.0	pF
Noise figure (I_C=1 mA dc, V_{CE}=6V dc, f=60 MHz R_S=400 ohms)	NF		6.0	dB

Matching characteristics	Symbol	Min	Max	Unit
D.C. current Gain Ratio (I_C= 1mA dc, V_{CE}=5V dc)	h_{FE1}/h_{FE2}	0.8	1.0	
Base voltage differential (I_C=1mA dc, V_{CE} = 5V dc.)	$\lvert V_{BE1}-V_{BE2}\rvert$		10	mV dc
Base voltage differential change (I_C = 1mA dc, V_{CE}=5V dc T_A= -55 to + 125°c)	$\frac{\Delta(V_{BE1}- V_{BE2})}{\Delta T_A}$		20	uV/^oC

2N3638 Fairchild PNP high current switches. High Beta h_{FE} 100 (min) @ I_C =50 mA. High current upto 500mA.

Maximum ratings: Storage temperature -55°C to + 125°C.

Operating junction temperature + 125°C maximum.

Maximum power dissipation 0.7 watt.

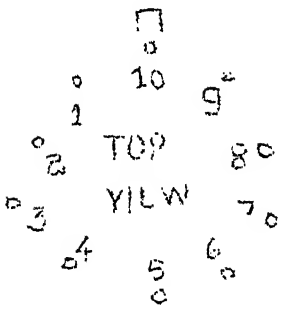
Maximum voltage and current

V_{CBO}	Collector to Base Voltage	-25 Volts
V_{CES}	Collector to emitter voltage	-25 volts.
V_{EBO}	Emitter to Base voltage	-4.0 volts
I_C	Collector current	500mA.

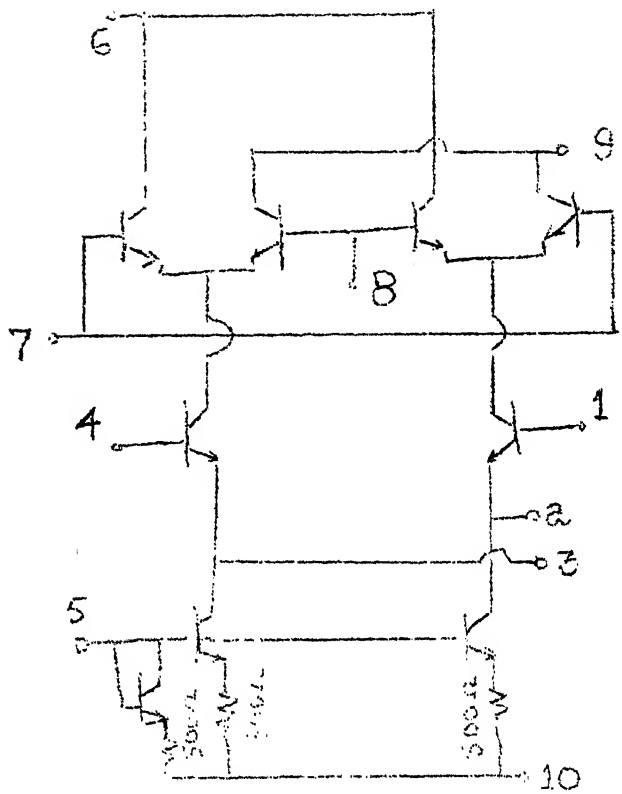
μA796C: Fairchild double balanced modulator Demodulator chip.

Pin connections

μA796



Schematic diagram



Maximum ratings:

Internal power dissipation	500 mW
Applied voltage (Note X)	30V
Differential input signal (V_7-V_8)	± 5.0V
Differential input signal (V_4-V_1)	± 5.0V
Input signal (V_2-V_1, V_3-V_4)	5.0V
Bias current I_5	12mA

(VI+VI)

Operating temperature range -65°C to +150°C

Note X: Voltage applied between pins 6-7, 8-1, 9-7, 9-8, 7-4, 7-1, 8-4, 6-8, 2-5, 3-5.

Electrical characteristics:

Transadmittance bandwidth	R_L=50 ohms		300 MHz
Input resistance	f=5.0MHz V_7-V_8=0.5Vdc		200KΩ
Input capacitance	f=5.0MHz V_7-V_8=0.5V dc		2.0 pF
Input bias current:	$(I_1+I_4)/2$	Min 12	Typ. 25 μA
Input bias current:	$(I_7+I_8)/2$	12	25 μA
Input off-set current:	(I_1-I_4)	0.7	5.0 μA
Input offset current :	(I_7-I_8)	0.7	5.0 μA
+ ve supply current :	(I_6+I_9)	2.0	3.0 mA
- ve supply current :	I_{10}	3.0	4.0 mA
Power dissipation			33 mW